

PRODUCT SPECIFICATION

8223A-SR

Wi-Fi Dual-band 1x1 11ac+ Bluetooth 5.0

Combo Module

Version:v1.7



8223A-SR Module Datasheet

	Part NO.	Description
Ordering Information	FG1023SM13-W2	QCA1023-0/QCA9377-3, a/b/g/n/ac Wi-Fi+BLE5.0, 1T1R, 12X12mm SDIO+Uart, V1.0
	FG1023SM13-K2	QCA1023-0/QCA9377-3, a/b/g/n/ac Wi-Fi+BLE5.0, 1T1R, 12X12mm SDIO+Uart, V1.0(Customer supply IC)
	FG1023SM13-W3	QCA1023-0/QCA9377-3, a/b/g/n/ac Wi-Fi+BLE5.0, 1T1R, 12X12mm SDIO+Uart, V1.0(GXX 版)

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL:+86-755-2955-8186

Website:www.fn-link.com

CONTENTS

1. General Description	6
1.1 Introduction	6
1.2 Description	6
2. Features	7
3. Block Diagram	7
4. General Specification	8
4.1 2.4GHz WI-FI Specification	8
4.2 5GHz WI-FI Specification	9
4.3 Bluetooth Specification	11
5. ID setting information	12
6. Pin Definition	13
6.1 Pin Outline	13
6.2 Pin Definition details	13
7. Electrical Specifications	15
7.1 Power Supply DC Characteristics	15
7.2 Power Consumption	16
7.3 Power sequencing	16
7.3.1 Case 1: 3.3 V power down after 1.8 V	16
7.3.2 Case 2: 1.8 V power down after 3.3 V	17
7.3.3 Case 3: All power rails supplied with 3.3 V	18
7.4 Host Interface Timing Diagram	19
7.4.1 SDIO Pin Description	19
7.4.2 SDIO Default Mode Timing Diagram	20
7.4.3 SDIO High Speed Mode Timing Diagram	21
7.4.4 SDIO Bus Timing Specifications in SDR Modes	21
7.4.5 SDIO Bus Timing Specifications in DDR50 Mode	24
8. Size reference	25
8.1 Module Picture	25
8.2 Marking Description	25
8.3 Physical Dimensions	26
8.4 Layout Recommendation	28
9. The Key Material List	28
10. Reference Design	29
10.1 External 32KHz clock SPEC	29
11. Recommended Reflow Profile	30
12. RoHS compliance	30
13. Package	31

13.1 Reel	31
13.2 Carrier Tape Detail	31
13.3 Packaging Detail	31
14. Moisture sensitivity	33

FN-LINK 欧智通

Revision History

1. General Description

1.1 Introduction

FN-Link Technology would like to announce a low-cost and low-power consumption module which has all of the Wi-Fi, Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11a/b/g/n/ac Access Points in the wireless LAN.

The wireless module complies with IEEE 802.11 a/b/g/n/ac standard and it can achieve up to a speed of 433.3Mbps with single stream in 802.11ac draft to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi, UART / PCM interface for Bluetooth.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

1.2 Description

Model Name	8223A-SR
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 12 x 12 x 1.7mm (typical)
Wi-Fi Interface	Support SDIO V3.0
BT Interface	UART / PCM
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	-40°C to 85°C
Storage temperature	-40°C to 125°C

1.-40 to 70°C range,the module is IEEE compliant.-40 to 85° C range, The module retains the ability to transmit data. Some parameters might decrease or exceed the specifications. When the temperature remains to normal levels, the module will meet IEEE specifications again.

2. Features

General

- Highly integrated wireless local area network(WLAN) system-on-chip (SOC) for 5 GHZ 802.11ac, or 2.4G/5G 802.11n WLAN applications.
- Supports 20/40MHz at 2.4GHz and supports 20/40/80MHz at 5GHz

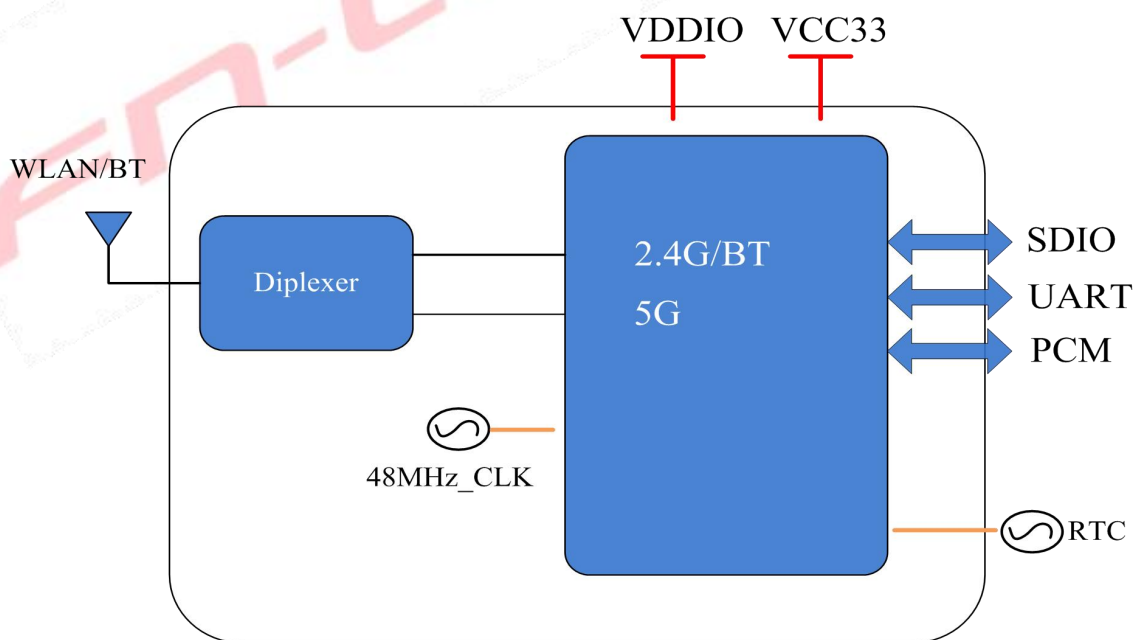
Host Interface

- Supports low power SDIO3.0 interface for WLAN and UART/PCM interface for Bluetooth

Bluetooth Features

- Supports Bluetooth V5.0, BLE and be backwards compatible with Bluetooth 1.2, 2.X+ enhance data rate
- Supports WLAN-Bluetooth coexistence
- Supports Bluetooth for class1 and class2 power level transmissions without requiring an external PA
- BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data

3. Block Diagram



4. General Specification

4.1 2.4GHz WI-FI Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz: Ch1 ~ Ch14	
Test Items	Typical Value	EVM
Output Power	802.11b /11Mbps : 16dBm ± 2 dB	EVM ≤ -9dB
	802.11g /54Mbps : 15dBm ± 2dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps PER @ -96 dBm	≤-83
	- 2Mbps PER @ -90 dBm	≤-80
	- 5.5Mbps PER @ -88 dBm	≤-79
	- 11Mbps PER @ -87 dBm	≤-76
Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps PER @ -90 dBm	≤-85
	- 9Mbps PER @ -88 dBm	≤-84
	- 12Mbps PER @ -87 dBm	≤-82
	- 18Mbps PER @ -85 dBm	≤-80
	- 24Mbps PER @ -83 dBm	≤-77
	- 36Mbps PER @ -80 dBm	≤-73
	- 48Mbps PER @ -76 dBm	≤-69
	- 54Mbps PER @ -74 dBm	≤-68
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -89 dBm	≤-85
	- MCS=1 PER @ -85 dBm	≤-82
	- MCS=2 PER @ -84 dBm	≤-80
	- MCS=3 PER @ -80 dBm	≤-77
	- MCS=4 PER @ -77 dBm	≤-73
	- MCS=5 PER @ -75 dBm	≤-69
	- MCS=6 PER @ -72 dBm	≤-68
	- MCS=7 PER @ -71 dBm	≤-67
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 PER @ -89 dBm	≤-82
	- MCS=1 PER @ -85 dBm	≤-79
	- MCS=2 PER @ -84 dBm	≤-77
	- MCS=3 PER @ -80 dBm	≤-74

- MCS=4	PER @ -76 dBm	≤-70
- MCS=5	PER @ -72 dBm	≤-66
- MCS=6	PER @ -70 dBm	≤-65
- MCS=7	PER @ -69 dBm	≤-64

4.2 5GHz WI-FI Specification

Feature	Description	
WLAN Standard	IEEE 802.11a/n/ac, Wi-Fi compliant	
Frequency Range	4.900 GHz ~ 5.845 GHz (5.0 GHz ISM Band)	
Number of Channels	5.0GHz: Please see the table1	
Modulation	802.11a/n : 64-QAM,16-QAM, QPSK, BPSK 802.11ac : 256-QAM, 64-QAM,16-QAM, QPSK, BPSK	
Output Power	802.11a /54M: 12 dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7: 11 dBm ± 2 dB	EVM ≤ -28dB
	802.11ac/MCS8: 10 dBm ± 2 dB	EVM ≤ -30dB
	802.11ac/MCS9: 10 dBm ± 2 dB	EVM ≤ -32dB
Test Items	Test Value	Standard Value
Receive Sensitivity (11a, 20MHz)@10% PER	- 6Mbps PER @ -91 dBm	≤-85
	- 9Mbps PER @ -89 dBm	≤-84
	- 12Mbps PER @ -88 dBm	≤-82
	- 18Mbps PER @ -86 dBm	≤-80
	- 24Mbps PER @ -82 dBm	≤-77
	- 36Mbps PER @ -79 dBm	≤-73
	- 48Mbps PER @ -74 dBm	≤-69
	- 54Mbps PER @ -73 dBm	≤-68
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -90 dBm	≤-85
	- MCS=1 PER @ -88 dBm	≤-82
	- MCS=2 PER @ -85 dBm	≤-80
	- MCS=3 PER @ -82 dBm	≤-77
	- MCS=4 PER @ -78 dBm	≤-73
	- MCS=5 PER @ -74 dBm	≤-69
	- MCS=6 PER @ -72 dBm	≤-68

	- MCS=7	PER @ -71 dBm	≤-67
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0	PER @ -88 dBm	≤-85
	- MCS=1	PER @ -85 dBm	≤-82
	- MCS=2	PER @ -83 dBm	≤-80
	- MCS=3	PER @ -79 dBm	≤-76
	- MCS=4	PER @ -76 dBm	≤-73
	- MCS=5	PER @ -71 dBm	≤-68
	- MCS=6	PER @ -70 dBm	≤-67
	- MCS=7	PER @ -68 dBm	≤-65
Receive Sensitivity (11ac,20MHz)@10% PER	- MCS=0	PER @ -89 dBm	≤-83
	- MCS=1	PER @ -87 dBm	≤-82
	- MCS=2	PER @ -84 dBm	≤-80
	- MCS=3	PER @ -81 dBm	≤-75
	- MCS=4	PER @ -77 dBm	≤-72
	- MCS=5	PER @ -73 dBm	≤-68
	- MCS=6	PER @ -71 dBm	≤-67
	- MCS=7	PER @ -70 dBm	≤-62
Receive Sensitivity (11ac,40MHz)@10% PER	- MCS=8	PER @ -66 dBm	≤-60
	- MCS=0	PER @ -87 dBm	≤-80
	- MCS=1	PER @ -83 dBm	≤-77
	- MCS=2	PER @ -81 dBm	≤-74
	- MCS=3	PER @ -78 dBm	≤-70
	- MCS=4	PER @ -75 dBm	≤-69
	- MCS=5	PER @ -70 dBm	≤-65
	- MCS=6	PER @ -68 dBm	≤-64
	- MCS=7	PER @ -66 dBm	≤-59
- MCS=8	PER @ -64 dBm	≤-57	
Receive Sensitivity (11ac,80MHz)@10% PER	- MCS=9	PER @ -63 dBm	≤-55
	- MCS=0	PER @ -83 dBm	≤-79
	- MCS=1	PER @ -80 dBm	≤-76
	- MCS=2	PER @ -78 dBm	≤-74
	- MCS=3	PER @ -74 dBm	≤-71
	- MCS=4	PER @ -71 dBm	≤-67
	- MCS=5	PER @ -69 dBm	≤-63
	- MCS=6	PER @ -65 dBm	≤-62
- MCS=7	PER @ -63 dBm	≤-61	

	- MCS=8	PER @ -60 dBm	≤-56
	- MCS=9	PER @ -59 dBm	≤-54

15GHz Channel table

Band (GHz)	Operating Channel Numbers	Channel center frequencies(MHz)
5.15GHz~5.25GHz	36	5180
	40	5200
	44	5220
	48	5240
5.25GHz~5.35GHz	52	5260
	56	5280
	60	5300
	64	5320
5.5GHz~5.7GHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
5.725GHz~5.825GHz	140	5700
	149	5745
	153	5765
	157	5785
	161	5805
	165	5825

4.3 Bluetooth Specification

Feature	Description
General Specification	
Bluetooth Standard	Bluetooth V5.0 ,BLE
Host Interface	UART

Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, $\pi/4$ -DQPSK, 8-DPSK		
RF Specification			
	Min(dBm)	Typical(dBm)	Max(dBm)
Output Power (Class 1)	2	5	15
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-92	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-92	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-85	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

5. ID setting information

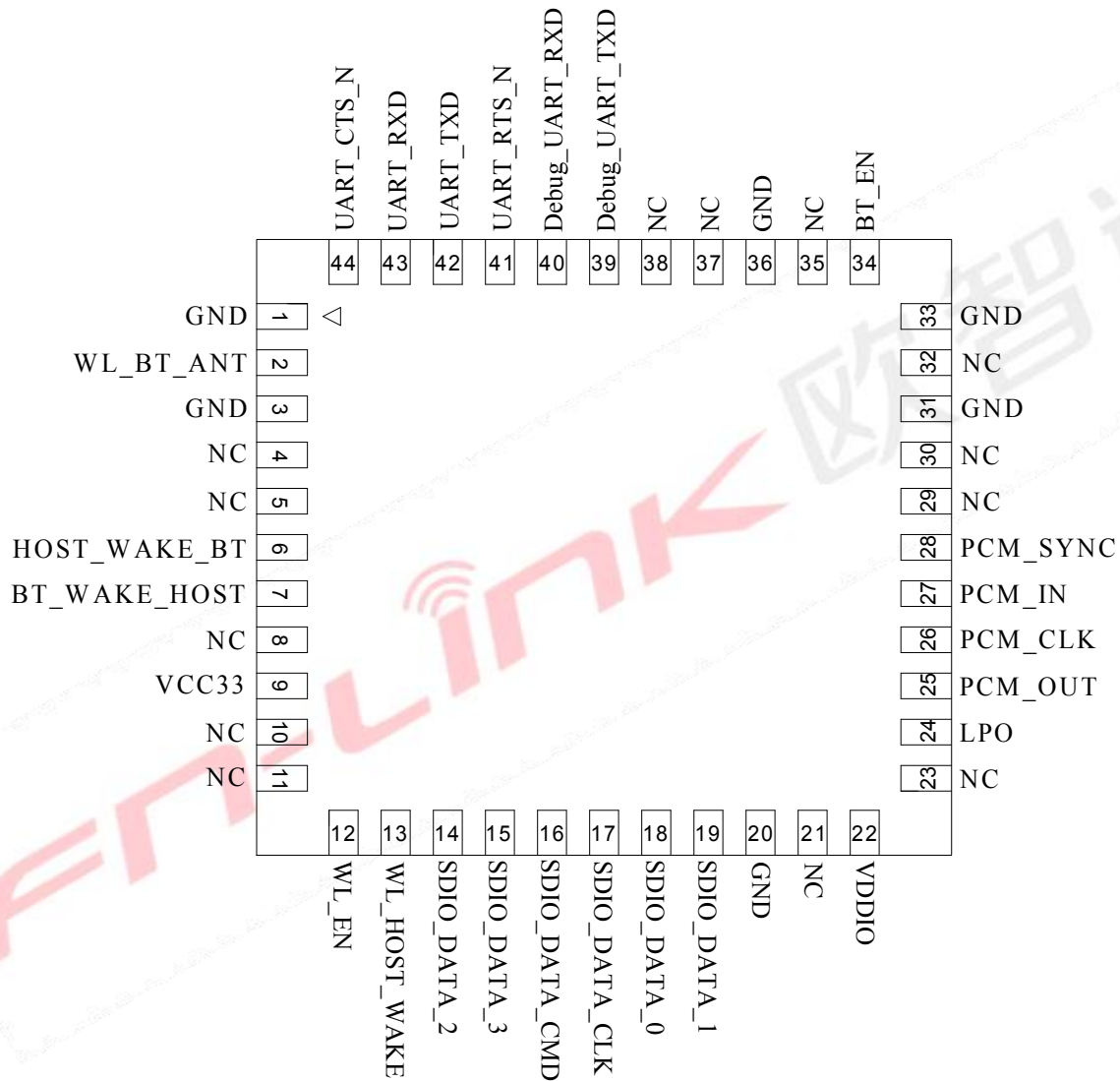
WI-FI

Vendor ID	0271
Product ID	0701

6. Pin Definition

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND	—	Ground connections	
2	WL_BT_ANT	I/O	RF I/O port	
3	GND	—	Ground connections	

4	NC	—	Floating (Don't connected to ground)	
5	NC	—	Floating (Don't connected to ground)	
6	HOST_WAKE_BT	I	HOST to wake-up Bluetooth device (IC pin55 :3D_FRAME_SYNC)	1.8V or 3.3V
7	BT_WAKE_HOST	O	Bluetooth device to wake-up HOST, Active high (IC pin93 :HCI_UART_WAKEHOST)	1.8V or 3.3V
8	NC	—	Floating (Don't connected to ground)	
9	VCC33	P	Main power voltage source input 3.3V	3.3V
10	NC	—	Floating (module pin is GND)	
11	NC	—	Floating (Don't connected to ground)	
12	WL_EN	I	Enable pin for WLAN device ON: pull high ; OFF: pull low	1.8V or 3.3V
13	WL_HOST_WAKE	O	WLAN to wake-up HOST (IC pin92:QOW)	1.8V or 3.3V
14	SDIO_DATA_2	I/O	SDIO data line 2, this pin must pull high 10KΩ resistor to VDDIO in main board.	1.8V or 3.3V
15	SDIO_DATA_3	I/O	SDIO data line 3	1.8V or 3.3V
16	SDIO_DATA_CMD	I/O	SDIO command line	1.8V or 3.3V
17	SDIO_DATA_CLK	I/O	SDIO clock line	1.8V or 3.3V
18	SDIO_DATA_0	I/O	SDIO data line 0	1.8V or 3.3V
19	SDIO_DATA_1	I/O	SDIO data line 1	1.8V or 3.3V
20	GND	—	Ground connections	1.8V or 3.3V
21	NC	—	Floating (Don't connected to ground) (IC pin48 :CLK_REQ)	
22	VDDIO	P	I/O Voltage supply input 1.8V or 3.3V	3.3V or 1.8V
23	NC	—	Floating (Don't connected to ground)	
24	LPO	I	External Low Power Clock input (32.768KHz)	1.8V or 3.3V
25	PCM_OUT	O	PCM Data output	1.8V or 3.3V
26	PCM_CLK	I/O	PCM clock	1.8V or 3.3V
27	PCM_IN	I	PCM data input	1.8V or 3.3V
28	PCM_SYNC	I/O	PCM sync signal	1.8V or 3.3V
29	NC	—	Floating (Don't connected to ground)	
30	NC	—	Floating (Don't connected to ground)	
31	GND	—	Ground connections	
32	NC	—	Floating (Don't connected to ground)	
33	GND	—	Ground connections	
34	BT_EN	I	Enable pin for Bluetooth device	1.8V or 3.3V

			ON: pull high ; OFF: pull low	
35	NC	—	Floating (Don't connected to ground)	
36	GND	—	Ground connections	
37	NC	—	Floating (Don't connected to ground)	
38	NC	—	Floating (Don't connected to ground)	
39	Debug_UART_TXD	O	Floating (Don't connected to ground) (IC pin61 :GPIO[19])	
40	Debug_UART_RXD	I	Floating (Don't connected to ground) (IC pin101 :GPIO[18])	
41	UART_RTS_N	O	Bluetooth UART interface	1.8V or 3.3V
42	UART_TXD	O	Bluetooth UART interface	1.8V or 3.3V
43	UART_RXD	I	Bluetooth UART interface	1.8V or 3.3V
44	UART_CTS_N	I	Bluetooth UART interface	1.8V or 3.3V

P:POWER I:INPUT O:OUTPUT

7. Electrical Specifications

7.1 Power Supply DC Characteristics

The digital IO supports VDD33 or VDD18 application.

	MIN	TYP	MAX	Unit
Operating Temperature	-40	25	85	deg.C
VCC33	3.15	3.3	3.45	V
VDDIO	1.7	1.8 or 3.3	3.45	V

Symbol	Min	Typ	Max	Unit
VIH	0.7xVDDIO	-	VDDIO+0.3	V
VIL	-0.3	-	0.3xVDDIO	V
VOH	0.9xVDDIO	-	VDDIO	V
VOL	0	-	0.1xVDDIO	V
IOH	3	-	-	mA
IOL	-	-	-11	mA
RPULL	-	1.8V IO: 120	-	kΩ

		3.3 IQ:70		
IIL	-5.0	-	5.0	μ A

7.2 Power Consumption

Power Consumption	VCC33 = 3.3V(Unit:mA)	
	Wi-Fi on Mode	72
TX (2.4G HT20)	220	
RX (2.4G HT20)	78	
TX (5G HT80)	220	
RX (5G HT80)	112	
BT on	20	

7.3 Power sequencing

7.3.1 Case 1: 3.3 V power down after 1.8 V

If the battery source can be removed from the end user device (battery removed, AC/DC plugged in), this is the recommended power sequence. It will avoid violating the power off sequence by allowing the 3.3 V rail to shut down after the 1.8 V rail.

Notes:

1. VDDIO_GPIO voltage should match VIO voltage from the host. In some applications, VDDIO_GPIO may be connected to 3.3 V upon Host VIO voltage.
2. In this case, both WLAN_EN and BT_EN on the QCA9377 are at 3.3 V due to using the VDD_AO power rail. If the host VIO voltage is 1.8 V, it must have level shifters to interface with host.
3. All host interface signals must stay floating or low before valid power on sequence (WLAN_EN and BT-EN goes high).

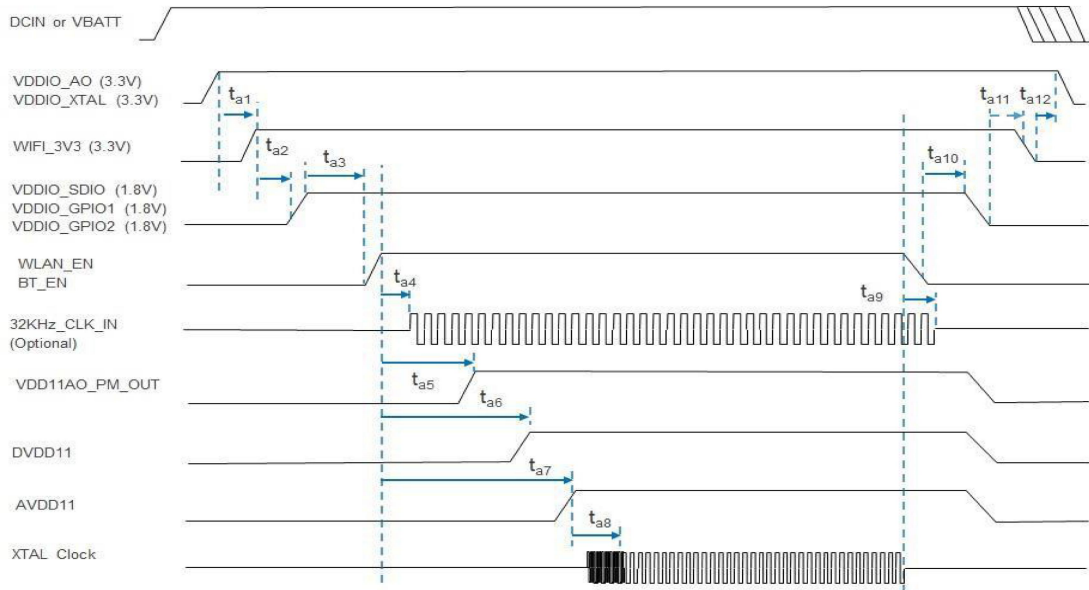


Figure 7-3-1 power sequence timing diagram (case 1)

power sequence timing table (case 1)

Symbol	Parameter	Min	Max	Units
t _{a1}	No requirement if VDDIO_AO connected to 3.3 V	0	—	μs
t _{a2}	90% of 3.3 V to 10% of 1.8 V	0	0	μs
t _{a3}	90% of VDDIO_GPIO to 0.7 V of both WLAN_EN and BT_EN	10	—	μs
t _{a4}	WLAN_EN valid to LF_CLK_IN input	0	—	μs
t _{a5}	WLAN_EN valid to VDD11AO_PM_OUT established	—	50	μs
t _{a6}	WLAN_EN to DVDD11	—	3.5	ms
t _{a7}	WLAN_EN to AVDD11	—	4	ms
t _{a8}	AVDD11 to XTAL clock stable	1	—	ms
t _{a9}	WLAN_EN de-assert (“low”) to LF_CLK_IN de-assert (tristate or	0	—	μs
t _{a10}	Both WLAN_EN = low and BT_EN = low to 90% of 1.8 V	10	—	μs
t _{a11}	3.3 V always higher than 1.8 V during operation, with power off by removing battery or unplugging AC/DC	0	—	μs
t _{a12}	VDDIO_AO and VDDIO_XTAL should be connected to 3.3 V power rail	0	—	μs

7.3.2 Case 2: 1.8 V power down after 3.3 V

If the battery source cannot be removed from the end user device, this is the recommended power sequence for this application. This sequence allows the software to control the power on/off sequence.

Notes:

1. VDDIO_GPIO voltage should match VIO voltage from the host. In some applications, VDDIO_GPIO may be connected to 3.3 V upon host VIO voltage.
2. Both WLAN_EN and BT_EN of QCA9377 are 1.8 V. If host VIO voltage is 1.8 V, it does not need level shifter to interface with host.
3. All host interface signals must stay floating or low before WLAN_EN/BT_EN = “high”, and after WLAN_EN/BT_EN = Low.

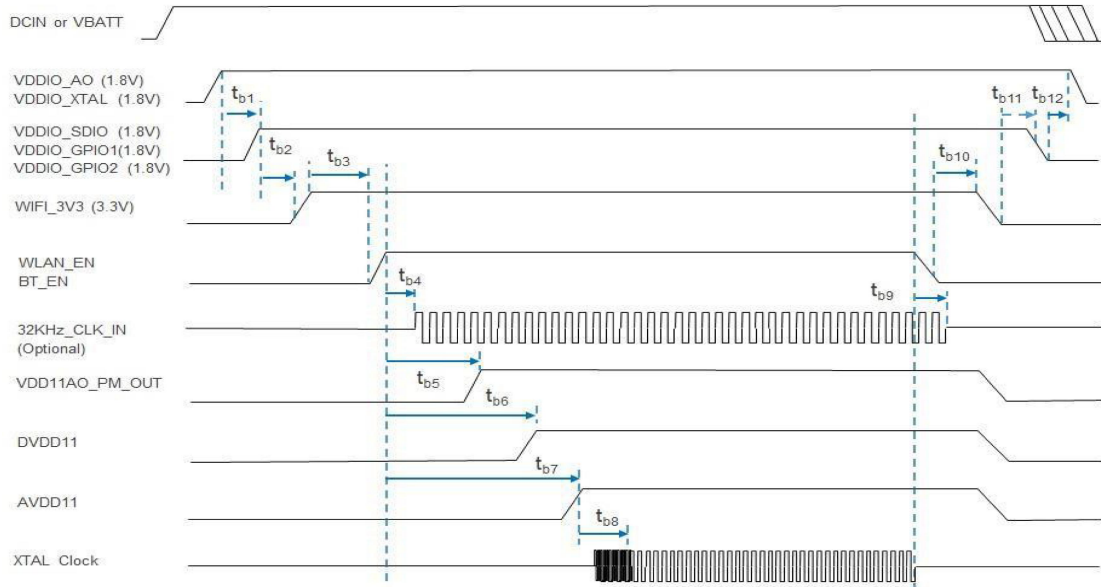


Figure 3-2 power sequence timing diagram (case 2)

Power sequence timing table (case 2)

Symbol	Parameter	Min	Max	Units
t _{b1}	No requirement if VDDIO_AO connected to 1.8 V	0	—	μs
t _{b2}	90% of 1.8 V to 10% of 3.3 V	0	—	μs
t _{b3}	90% of 3.3 V to 0.7 V of both WLAN_EN and BT_EN	10	—	μs
t _{b4}	WLAN_EN valid to LF_CLK_IN input	0	—	μs
t _{b5}	WLAN_EN valid to VDD11AO_PM_OUT established	—	50	μs
t _{b6}	WLAN_EN to DVDD11	—	3.	ms
t _{b7}	WLAN_EN to AVDD11		4	ms
t _{b8}	AVDD11 to XTAL clock stable	1	—	ms
t _{b9}	WLAN_EN de-assert (“low”) to LF_CLK_IN de-assert (tristate or low)	0	—	μs
t _{b10}	Both WLAN_EN = low and BT_EN = low to 90% of 3.3 V	10	—	μs
Symb	Parameter	Min	Max	Units
t _{b11}	10% of 3.3 V to 90% of 1.8 V	0	—	μs
t _{b12}	VDDIO_AO and VDDIO_XTAL should be connected to 1.8 V power	0	—	μs

7.3.3 Case 3: All power rails supplied with 3.3 V

All power pins are connected to 3.3 V only include VDDIO_AO, VDDIO_XTAL, VDDIO_GPIOx.

Note: All host signals are either GND or floating before WLAN_EN/BT_EN = ”high”, and after WLAN_EN/BT_EN = Low.

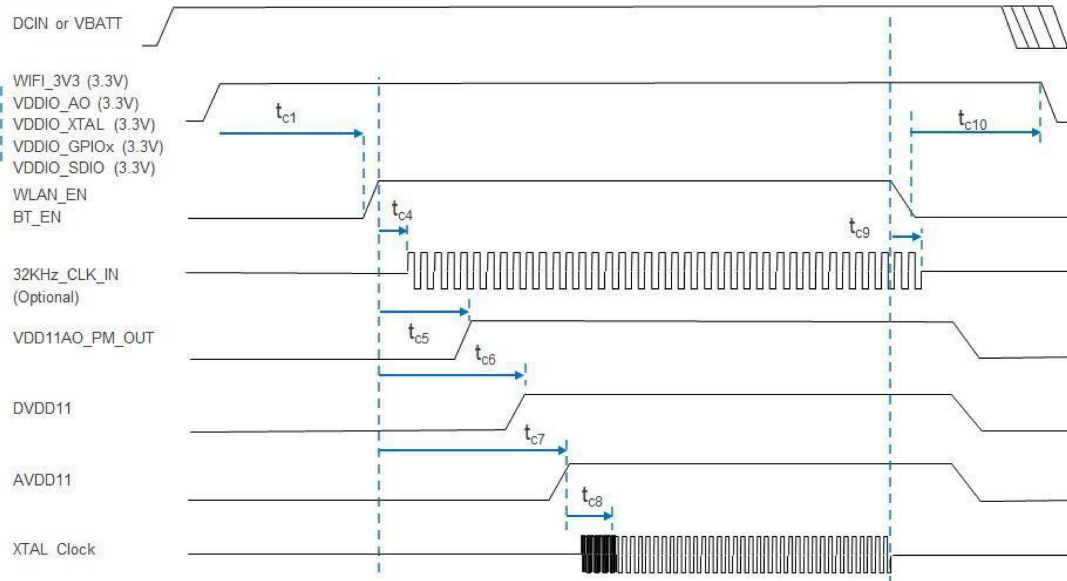


Figure 3-3 power sequence timing diagram (case 3)

Power sequence timing table (case 3)

Symbo	Parameter	Min	Max	Unit
t _{c1}	90% of 3.3 V to 0.7 V of both WLAN_EN and BT_EN	0	—	μs
t _{c4}	WLAN_EN valid to LF_CLK_IN input	0	—	μs
t _{c5}	WLAN_EN valid to VDD11AO_PM_OUT established	—	50	μs
t _{c6}	WLAN_EN to DVDD11	—	3	ms
t _{c7}	WLAN_EN to AVDD11	—	4	ms
t _{c8}	AVDD11 to XTAL clock stable	1	—	ms
t _{c9}	WLAN_EN de-assert (“low”) to LF_CLK_IN de-assert(tristate or low)	0	—	μs
t _{c10}	Both WLAN_EN = low and BT_EN = low to 90% of 3.3 V	10	—	μs

7.4 Host Interface Timing Diagram

7.4.1 SDIO Pin Description

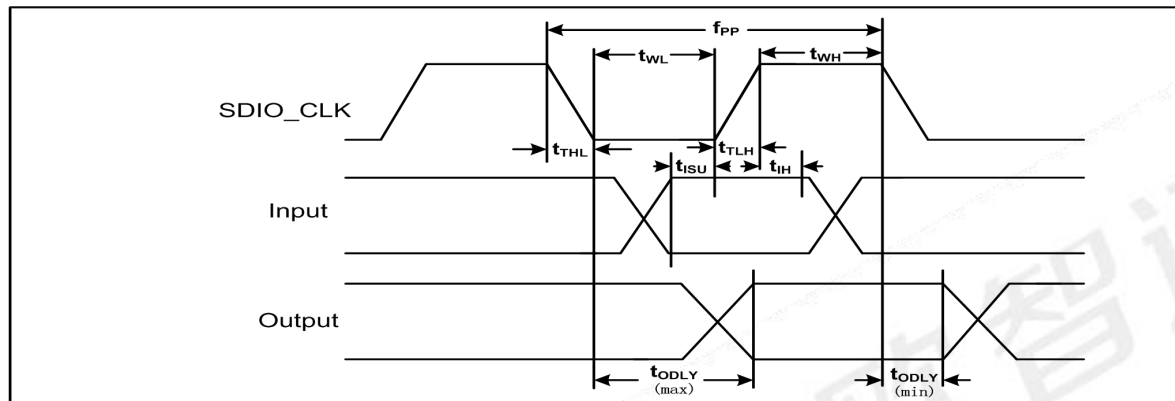
The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps), SDR104(208MHz) and DDR50(50MHz, dual rates) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This ‘out-of-band’ interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait

DATA3	Data Line 3
CLK	Clock
CMD	Command Line

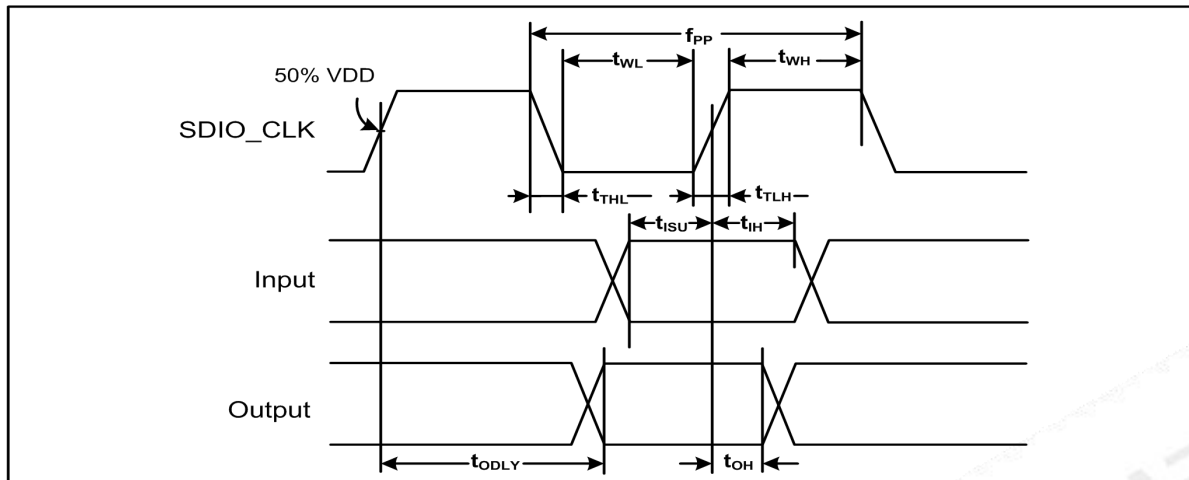
7.4.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK(All values are referred to minimum VIH and maximum VIL^b)					
Frequency - Data Transfer mode	fPP	0	-	25	MHz
Frequency - Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs:CMD, DAT(referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs:CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	0	-	14	ns
Output delay time - Identification mode	tODLY	0	-	50	ns

- a. Timing is based on $CL \leq 40$ pF load on CMD and Data.
- b. $Min(V_{ih}) = 0.7 \times V_{DDIO}$ and $max(V_{il}) = 0.2 \times V_{DDIO}$.

7.4.3 SDIO High Speed Mode Timing Diagram

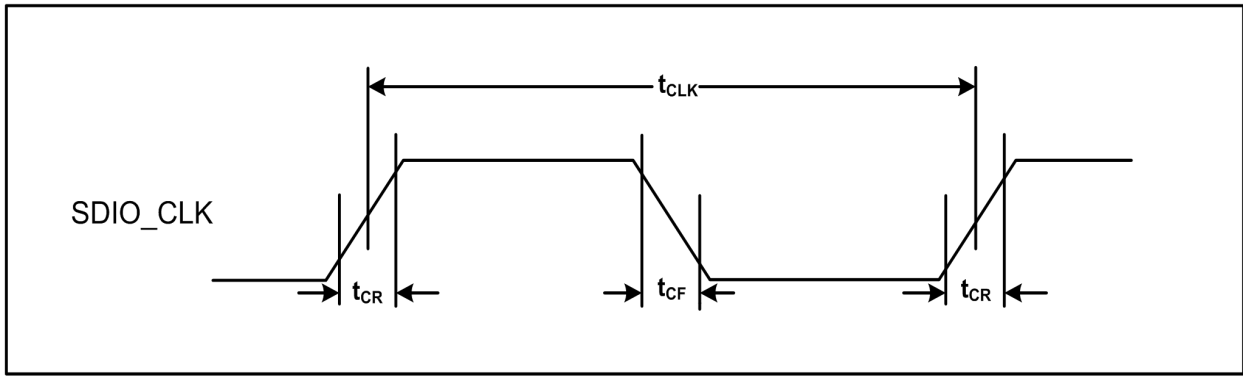


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK(all values are referred to minimum VIH and maximum VIL^b)					
Frequency - Data Transfer mode	fPP	0	-	50	MHz
Frequency - Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs:CMD, DAT(referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs:CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	-	-	14	ns
Output delay time - Identification mode	tODLY	2.5	-	-	ns
Total system capacitance(each line)	CL	-	-	40	pF

- a. Timing is based on $CL \leq 40$ pF load on CMD and Data.
- b. $\text{Min}(V_{ih}) = 0.7 \times V_{DDIO}$ and $\text{max}(V_{il}) = 0.2 \times V_{DDIO}$.

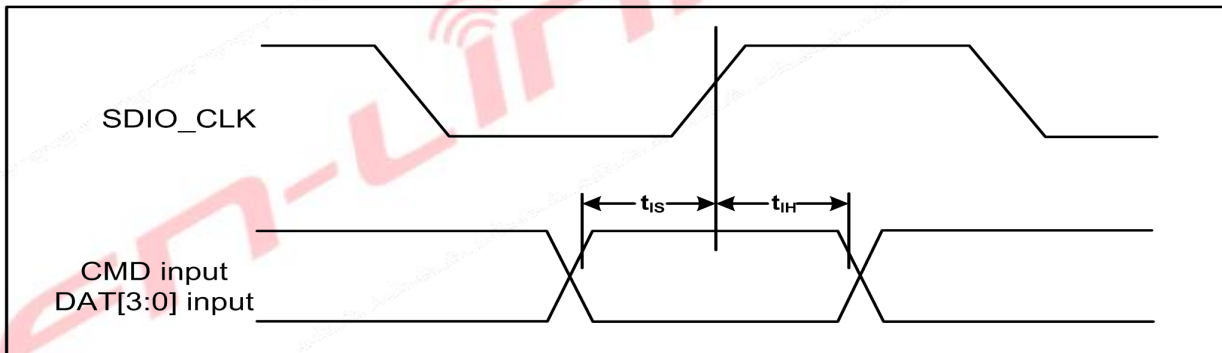
7.4.4 SDIO Bus Timing Specifications in SDR Modes

Clock timing(SDR Modes)



Parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t_{CLK}	40	-	ns	SDR12 mode
-		20	-	ns	SDR25 mode
-		10	-	ns	SDR50 mode
-		4.8	-	ns	SDR104 mode
-	t_{CR}, t_{CF}	-	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max)@100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max)@208 MHz, $C_{CARD} = 10$ pF
Clock duty	-	30	70	%	-

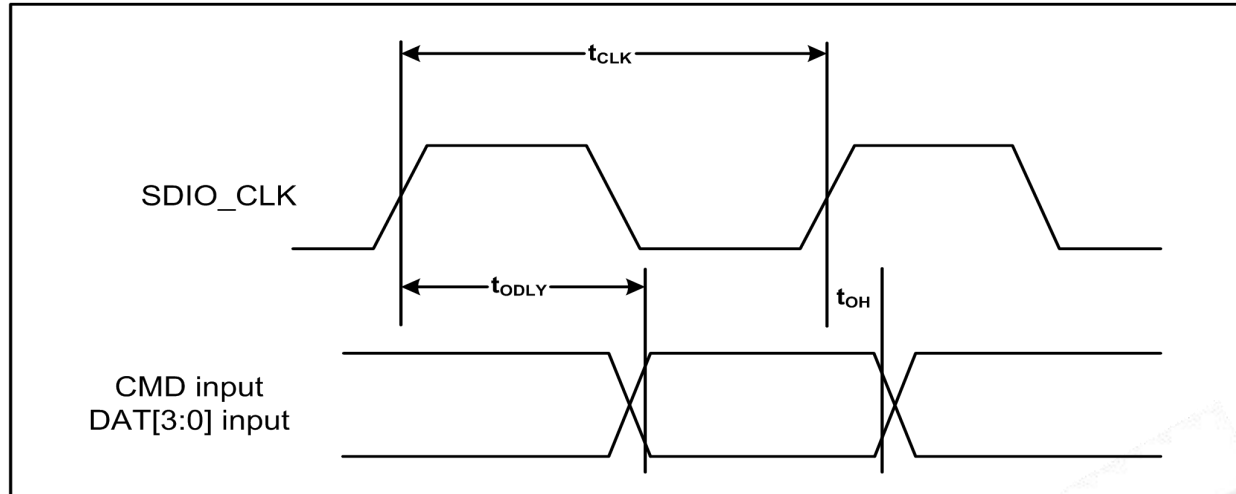
Card Input timing (SDR Modes)



Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.70 ^a	-	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	-	ns	$C_{CARD} = 5$ pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	-	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	-	ns	$C_{CARD} = 5$ pF, VCT = 0.975V

a. SDIO 3.0 specification value is 1.40 ns.

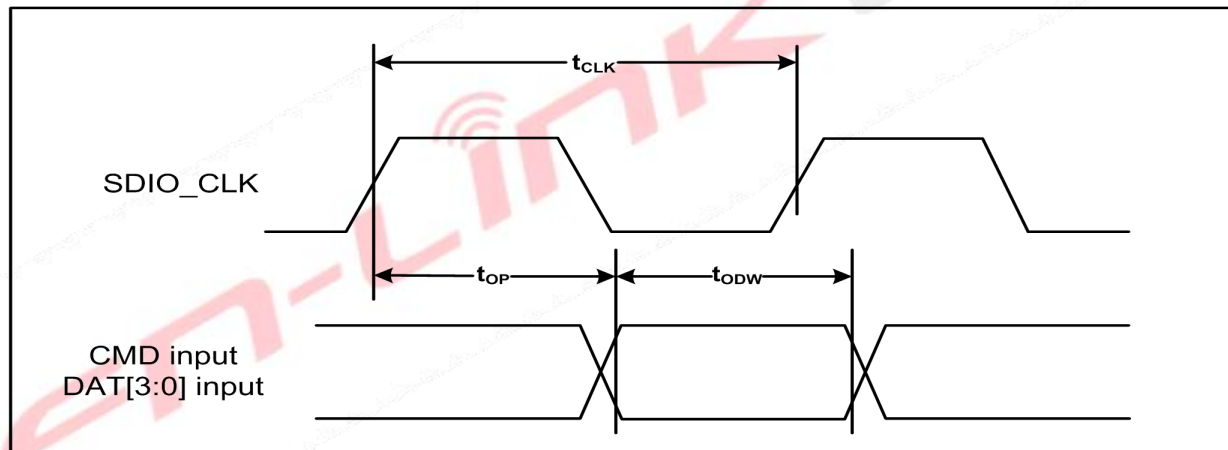
Card output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t _{ODLY}	-	7.85 ^a	ns	t _{CLK} ≥ 10 ns C _L = 30 pF using driver type B for SDR50
t _{ODLY}	-	14.0	ns	t _{CLK} ≥ 20 ns C _L = 40 pF using for SDR12, SDR25
t _{OH}	1.5	-	ns	Hold time at the t _{ODLY} (min) C _L = 15 pF

a. SDIO 3.0 specification value is 7.5 ns.

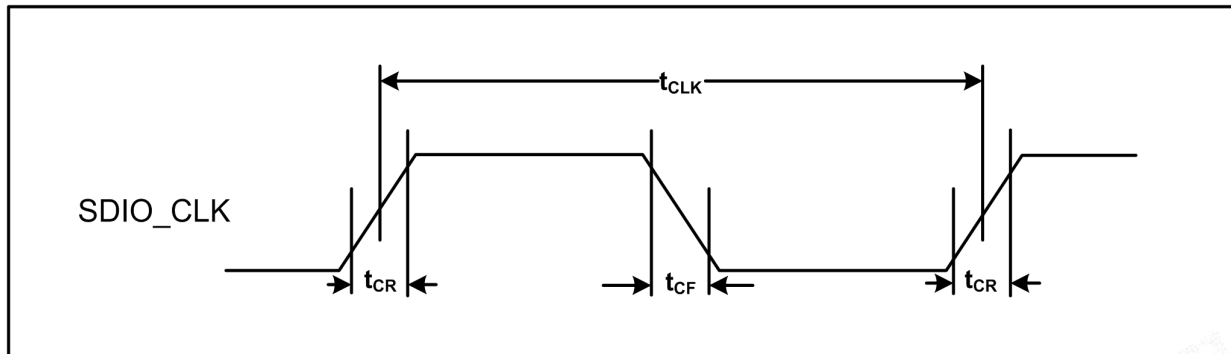
Card output timing (SDR Modes 100MHz to 208MHz)



Symbol	Minimum	Maximum	Unit	Comments
t _{OP}	0	2	UI	Card output phase
Δt _{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t _{ODW}	0.6	-	UI	t _{ODW} = 2.88 ns @ 208 MHz

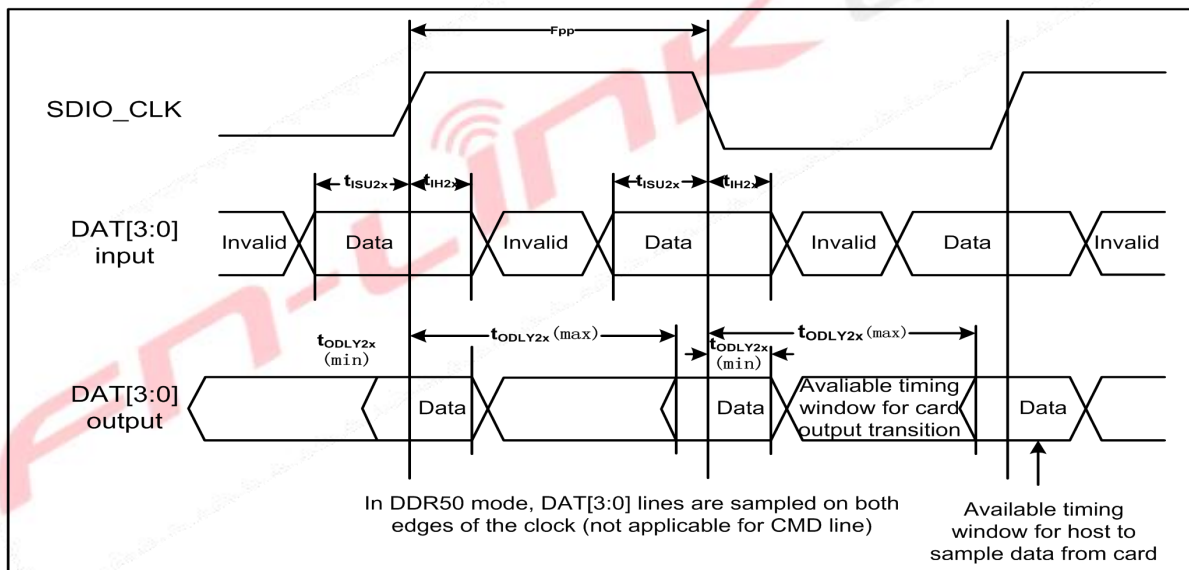
- Δt_{OP} = +1550 ps for junction temperature of Δt_{OP} = 90 degrees during operation
- Δt_{OP} = -350 ps for junction temperature of Δt_{OP} = -20 degrees during operation
- Δt_{OP} = +2600 ps for junction temperature of Δt_{OP} = -20 to +125 degrees during operation

7.4.5 SDIO Bus Timing Specifications in DDR50 Mode



parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t _{CLK}	20	-	ns	DDR50 mode
-	t _{CR} , t _{CF}	-	0.2 × t _{CLK}	ns	t _{CR} , t _{CF} < 4.00 ns (max)@50 MHz, C _{CARD} = 10 pF
Clock duty	-	45	55	%	-

Data Timing



parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t _{ISU}	6	-	ns	C _{CARD} < 10 pF (1 Card)
Input hold time	t _{IH}	0.8	-	ns	C _{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t _{ODLY}	-	13.7	ns	C _{CARD} < 30 pF (1 Card)
Output hold time	t _{OH}	1.5	-	ns	C _{CARD} < 15 pF (1 Card)

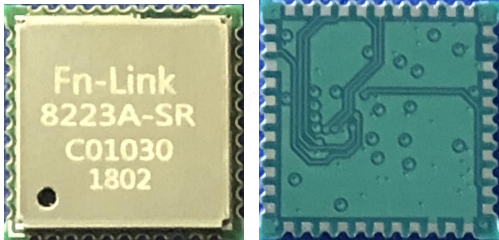
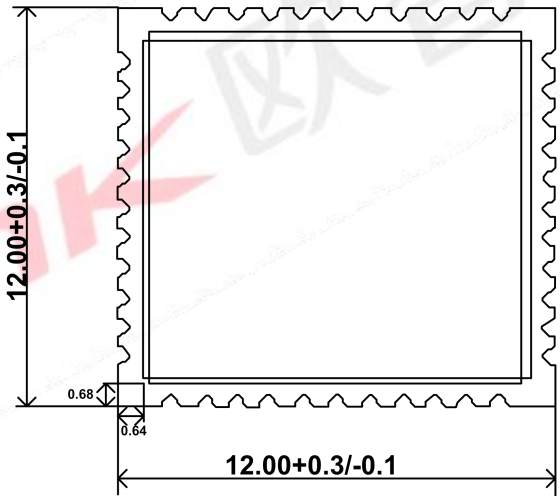
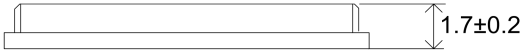
Input DAT

Input setup time	t_{ISU2x}	3	-	ns	$C_{CARD} < 10 \text{ pF (1 Card)}$
Input hold time	t_{IH2x}	0.8	-	ns	$C_{CARD} < 10 \text{ pF (1 Card)}$
Output CMD					
Output delay time	t_{ODLY2x}	-	7.85 ^a	ns	$C_{CARD} < 25 \text{ pF (1 Card)}$
Output hold time	t_{ODLY2x}	1.5	-	ns	$C_{CARD} < 15 \text{ pF (1 Card)}$

a. SDIO 3.0 specification value is 7.0 ns

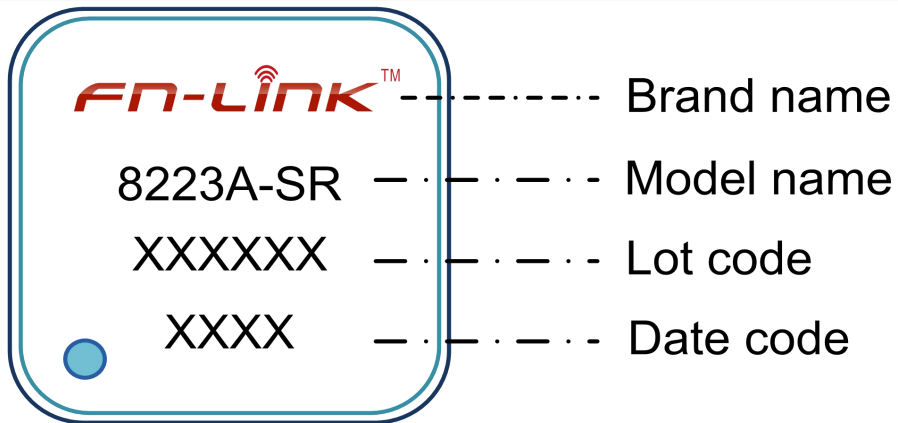
8. Size reference

8.1 Module Picture

<p>L x W : 12 x 12 (+0.3/-0.1) mm</p> 	
<p>H: 1.7 (±0.2) mm</p>	
<p>Weight</p>	<p>0.53g</p>

8.2 Marking Description

< TOP VIEW >



Datecode:

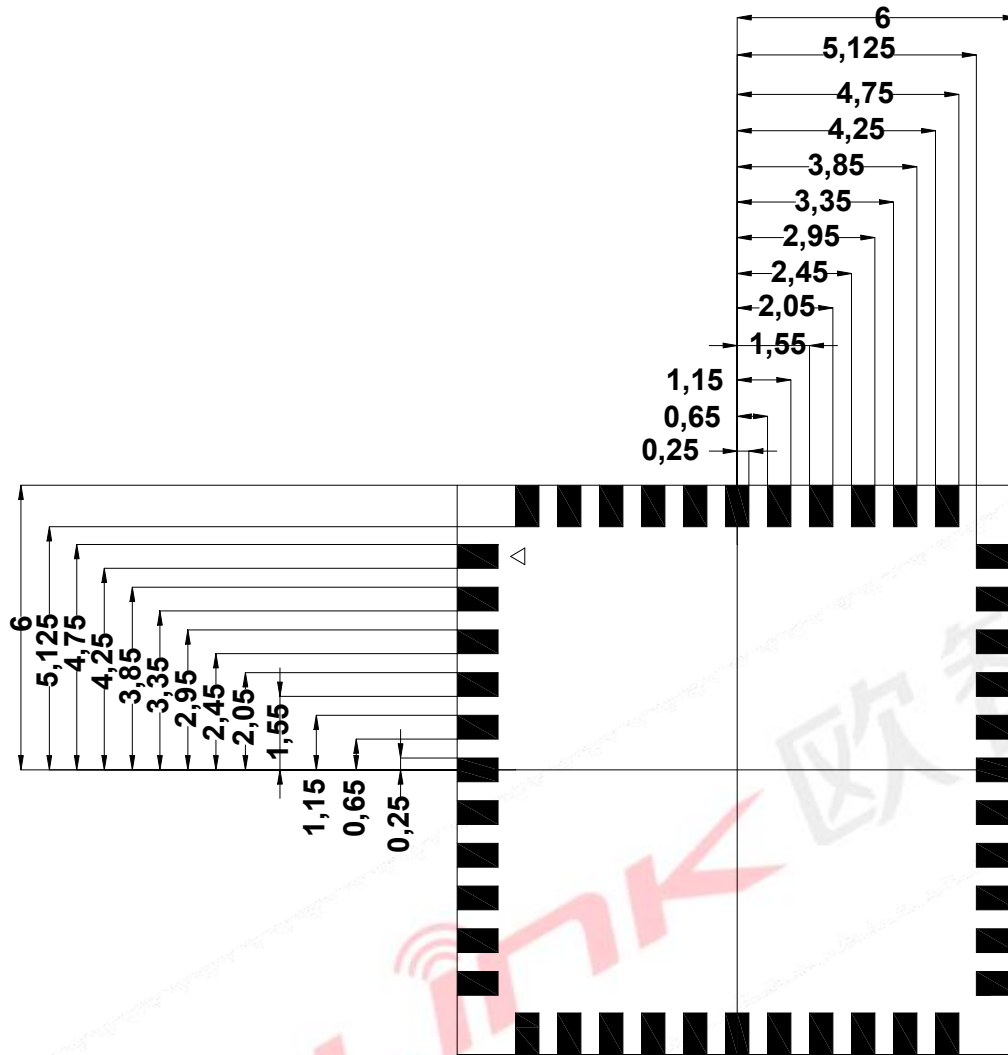
XXXX : -w2 model

XXXXK2: -K2 model

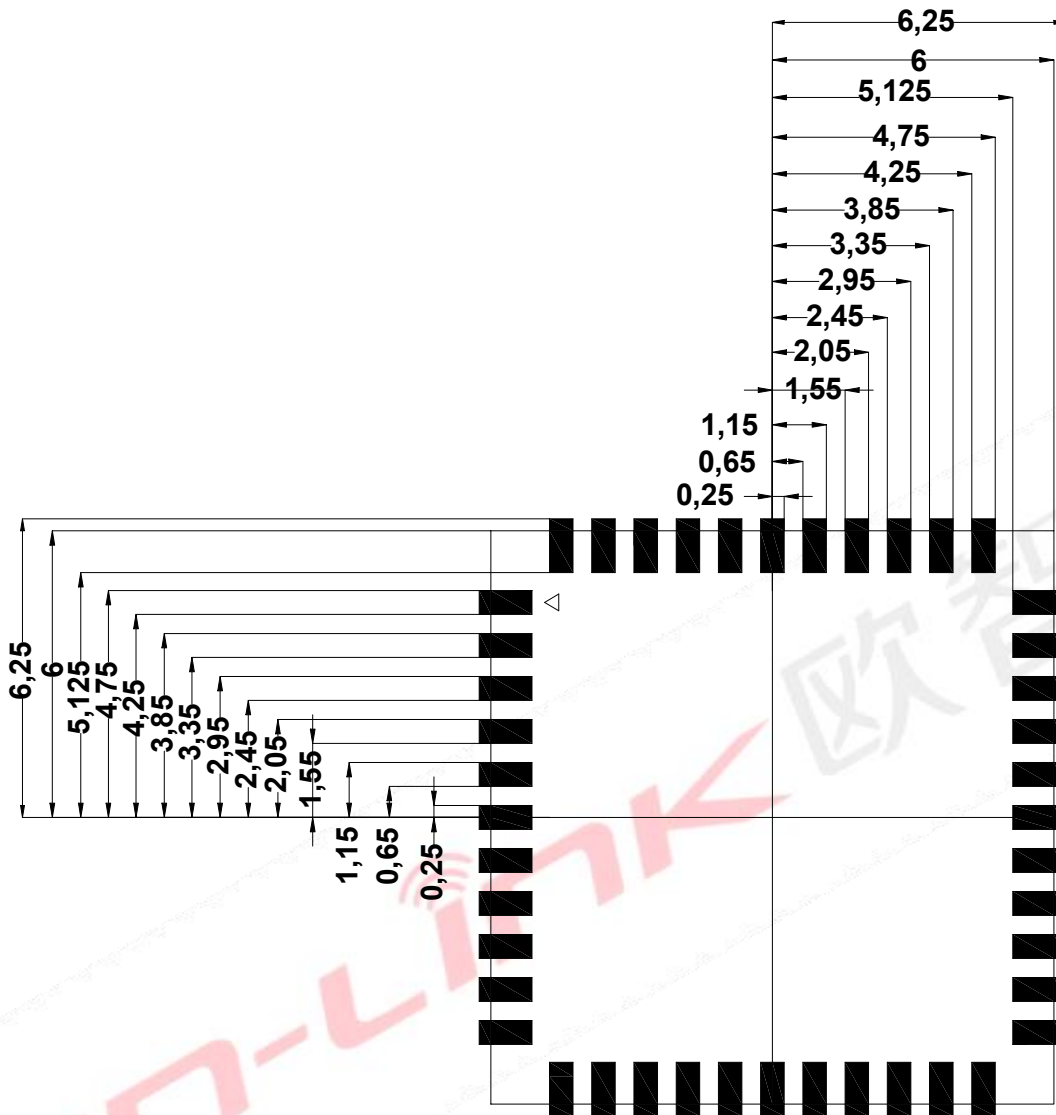
XXXXW3: -W3 model

8.3 Physical Dimensions

<TOP View>



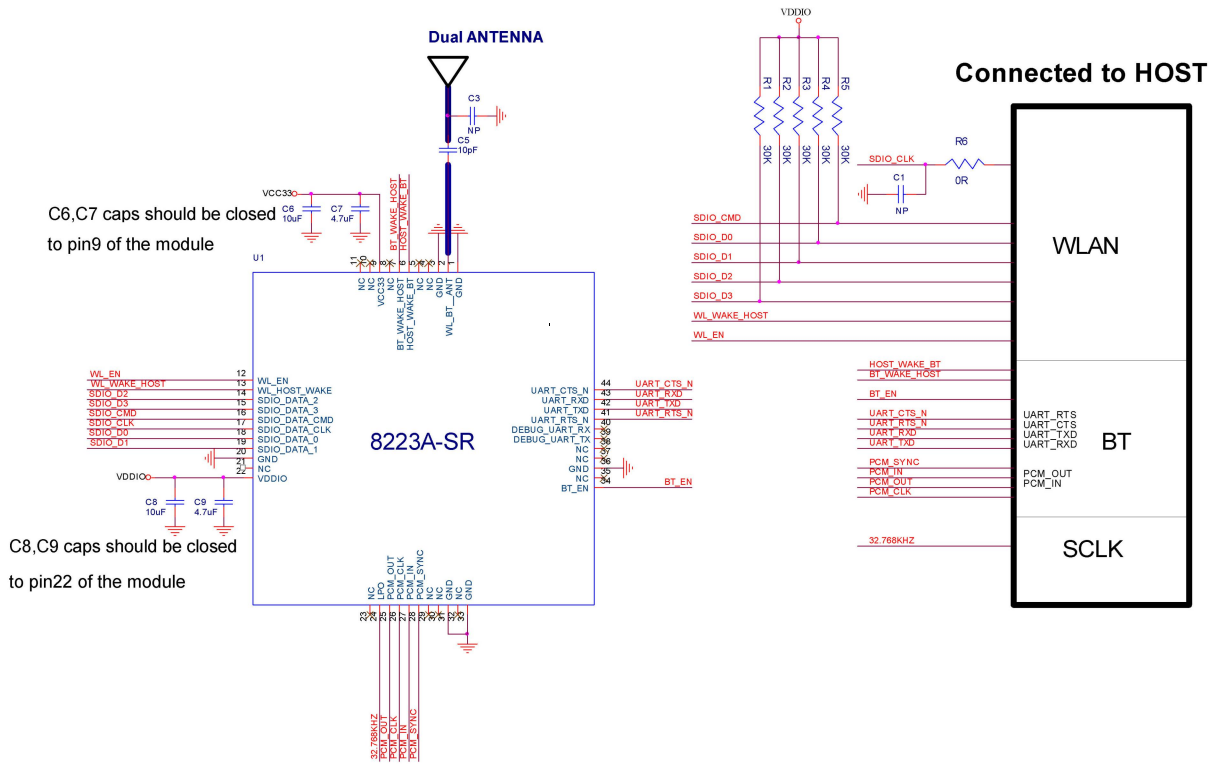
8.4 Layout Recommendation



9. The Key Material List

Item	Part Name	Description	Manufacturer
1	Inductor	2016 1.5uH, ±20%, 800mA	Microgate,Cenke,Ceaiya,sunlord
2	Crystal	2016 48MHZ 10ppm, 8.8pF	Hosonic,ECEC,TKD,JWT,TST,SIW ARD
3	Diplexer	Diplexer,1608,2.4G+5G	ACX,Wlsain,Glead,maglayers
4	Chipset	QCA1023-0/QCA9377-3	Qualcomm
5	Shielding	F1023XM13-W1 Shielding cover	精力通, 信太
6	PCB	8223A-SR Green,6L,12X12X0.498mm	Sunlord,Brainpower PCB,KX-PCB

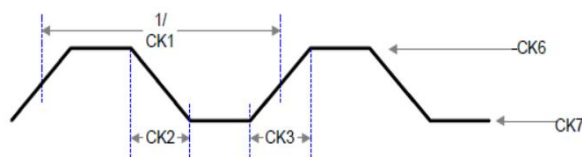
10. Reference Design



10.1 External 32KHz clock SPEC

- 1.The module does not require an external 32 kHz clock. By default, the WiFi chip set utilizes its internal 200 kHz clock shared with the WLAN and BT subsystem.
- 2.If the end application has a more accurate 32 kHz clock,the requirements are:

Symbol	Description	Min	Typ	Max	Unit
CK1	Clock rate	-	32.768	-	kHz
CK2	Fall time	1	-	100	ns
CK3	Rise time	1	-	100	ns
CK4	Duty cycle (high-to-low ratio)	15	-	85	%
CK5	Frequency stability	-200	-	200	ppm
CK6	Input high voltage	$0.8 \times VDDIO_GPIO2$	-	$VDDIO_GPIO2 + 0.2$	V
CK7	Input low voltage	-0.3	-	$0.2 \times VDDIO_GPIO2$	V

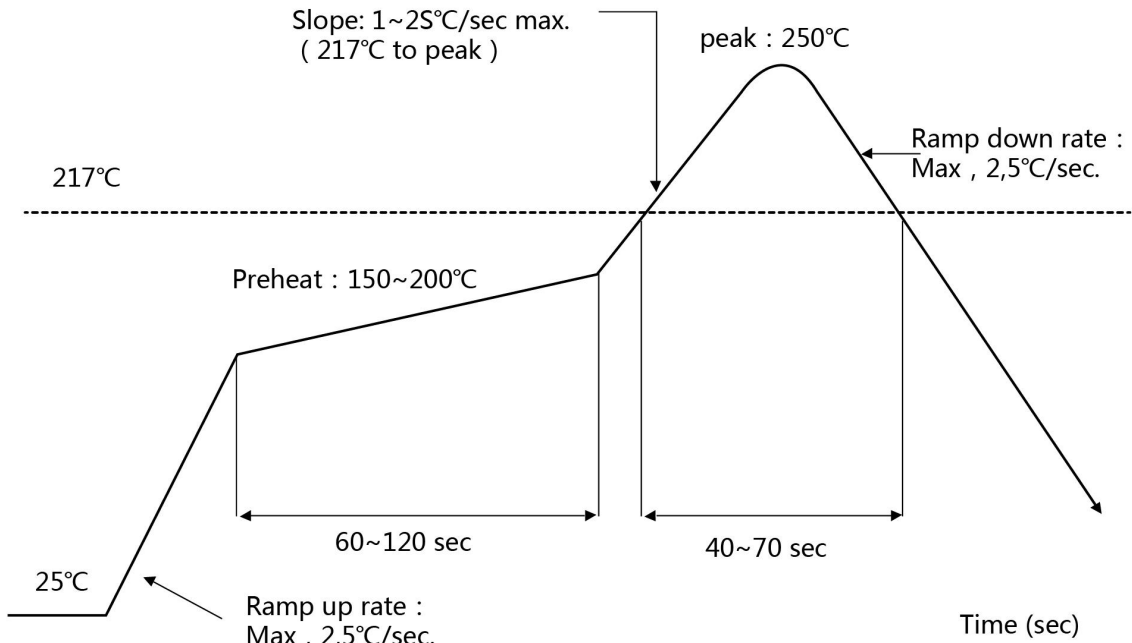


11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times



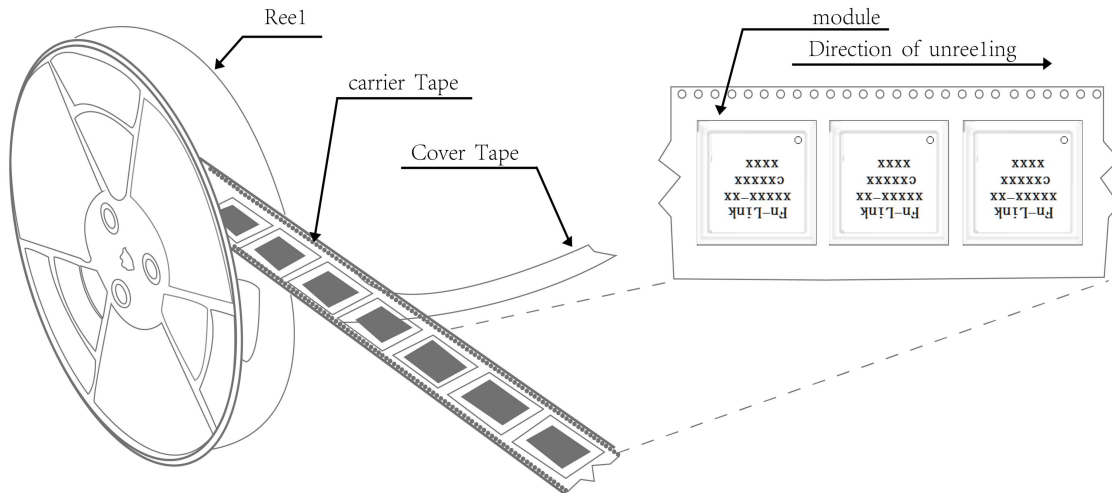
12. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

13. Package

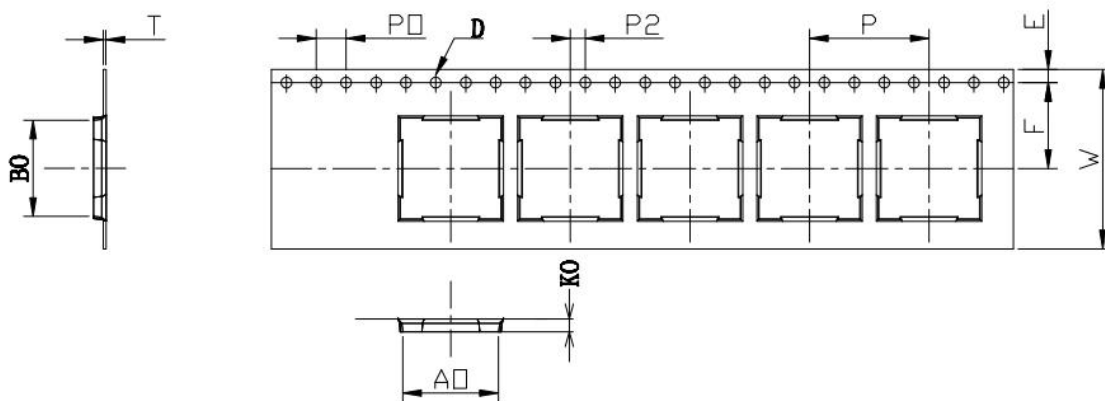
13.1 Reel

A roll of 1500pcs



13.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	12.45	12.45	1.50	11.5	1.75	2.60	4.0	2.0	16.0	0.30
TOLE	+0.3 -0.3	±0.10	±0.10	+0.1 -0.0	+0.1 -0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



13.3 Packaging Detail

the take-up package



Using self-adhesive tape

Size of black tape: 24mm*32.6m the cover tape :21.3mm*32.6m

Color of plastic disc: blue



NY bag size:450mm*415mm



size : 350*350*35mm



The packing case size:360*210*370mmg

14. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)
- b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
- c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- d) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected
- e) Baking is required if conditions b) or c) are not respected
- f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more

Appendix 1

Certification information

TELEC



CE

RE-18010505



FCC

FCC ID: 2AATL-8223A-SR

IC

24844-8223ASR

SRRC

CMIIT ID:2019AP11087(M)