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欧智通科技

Fn-Link

6223A-SRD

WiFi Single-band 1X1 +
Bluetooth v2.1+EDR/Bluetooth
3.0/3.0+HS/4.2

Module Datasheet

Revision History

Date	Revision Content	Revised By	Version
2016-9-26	First Released	William Tan	1.0
2016-12-19	Modified pin definition and BT version	Colin Ming	1.1
2017-02-10	Modified reference design	Colin Ming	1.2

CONTENTS

1. Introduction

6223A-SRD is a small size and low profile of WiFi + BT Combo module with LGA (Land-Grid Array) footprint, board size is 12mm*12mm with module thickness of 2mm. It can be easily manufactured on SMT process and highly suitable for tablet PC, ultra book, mobile device and consumer products. It provides SDIO interface for WiFi to connect with host processor and high speed UART interface for BT. It also has a PCM interface for audio data transmission with direct link to external audio codec via BT controller. The WiFi throughput can go up to 150Mbps in theory by using 1x1 802.11n b/g/n MIMO technology and Bluetooth can support BT2.1+EDR/BT3.0 and BT4.2.

6223A-SRD uses highly integrated WiFi/BT single chip based on advanced COMS process. 6223A-SRD integrates whole WiFi/BT function blocks into a chip, such as SDIO/UART, MAC, BB, AFE, RFE, PA, EEPROM and LDO/SWR, except fewer passive components remained on PCB.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

2. Features

- Operate at ISM frequency bands (2.4GHz)
- SDIO for WiFi and UART for Bluetooth
- IEEE standards support: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n, IEEE 802.11d, IEEE 802.11e, IEEE 802.11h, IEEE 802.11i
- Fully Qualified for Bluetooth 2.1+EDR specification including both 2Mbps and 3Mbps modulation mode
- Fully qualified for Bluetooth 3.0
- Fully qualified for Bluetooth 4.2 Dual mode
- Full–speed Bluetooth operation with Piconet and Scatternet support
- Enterprise level security which can apply WPA/WPA2 certification for WiFi.
- WiFi 1 transmitter and 1 receiver allow data rates supporting up to 150 Mbps downstream and 150 Mbps upstream PHY rates

3. General Specification

3.1 General Specification

Model Name	6223A-SRD
Product Description	Support WiFi/Bluetooth functionalities
Dimension	L x W x H: 12 x 12 x1.5 (typical) mm
WiFi Interface	Support SDIO V3.0
BT Interface	UART / PCM
Operating temperature	0°C to 70°C
Storage temperature	-40°C to 85°C

3.2 Recommended Operating Rating

	Min.	Typ.	Max.	Unit
Operating Temperature	0	25	70	deg.C
VCC33	3.15	3.3	3.45	V
VDDIO	1.7	1.8 or 3.3	3.45	V

4. WiFi/BT RF Specification

4.1 2.4GHz RF Specification

Feature	Description
Operating Frequency	2.400～2.4835GHz
Standards	WiFi: IEEE 802.11b, IEEE 802.11g, IEEE 802.11n, IEEE 802.11d, IEEE 802.11e, IEEE 802.11h, IEEE 802.11i BT: V2.1+EDR/BT v3.0/BT v3.0+HS/BT v4.2
Modulation	WiFi: 802.11b: CCK(11, 5.5Mbps), QPSK(2Mbps), BPSK(1Mbps), 802.11 g/n: OFDM BT: 8DPSK, π/4 DQPSK, GFSK
PHY Data rates	WiFi: 802.11b: 11,5.5,2,1 Mbps 802.11g: 54,48,36,24,18,12,9,6 Mbps 802.11n: up to 150Mbps BT: 1 Mbps for Basic Rate 2,3 Mbps for Enhanced Data Rate
Transmit Output Power	WiFi: 802.11b@11Mbps 16±1.5dBm 802.11g@54Mbps 14±1.5dBm 802.11n@65Mbps 13±1.5dBm (MCS 7_HT20) 13±1.5dBm (MCS 7_HT40) BT: Max +10dBm
EVM	802.11b /1Mbps : EVM≦-10dB 802.11b /11Mbps : EVM≦-10dB 802.11g /6Mbps : EVM≦-5dB 802.11g /54Mbps : EVM≦-25dB 802.11n /6.5Mbps : EVM≦-5dB 802.11n /65Mbps : EVM≦-28dB

	802.11n /13.5Mbps : EVM≦-5dB 802.11n /135Mbps : EVM≦-28dB
Receiver Sensitivity (WiFi)	802.11b@8% PER 1Mbps ≦-91dBm 2Mbps≦ -89dBm 5.5Mbps≦ -87dBm 11Mbps ≦-85dBm Max input level≥-8
	802.11g@10% PER 6Mbps ≦-87dBm 9Mbps ≦-86dBm 12Mbps≦ -84dBm 18Mbps≦ -82dBm 24Mbps≦ -79dBm 36Mbps≦ -75dBm 48Mbps ≦-71dBm 54Mbps ≦-70dBm Max input level≥-20
	802.11n@10% PER HT20_MCS 0 ≦-87dBm HT40_MCS 0≦-84 HT20_MCS 1≦ -84dBm HT40_MCS 1≦-81 HT20_MCS 2 ≦-82dBm HT40_MCS 2≦-79 HT20_MCS 3 ≦-79dBm HT40_MCS 3≦-76 HT20_MCS 4 ≦-75dBm HT40_MCS 4≦-72 HT20_MCS 5 ≦-71dBm HT40_MCS 5≦-68 HT20_MCS 6 ≦-70dBm HT40_MCS 6≦-67 HT20_MCS 7 ≦-69dBm HT40_MCS 7≦-66 Max input level≥-20
Receiver Sensitivity (BT)	-89dBm @ 1Mbps -86dBm @ 2Mbps -83dBm @ 3Mbps
Operating Channel	WiFi 2.4GHz: 11: (Ch. 1-11) – United States 13: (Ch. 1-13) – Europe 14: (Ch. 1-14) – Japan BT 2.4GHz: Ch. 0 ~78
Media Access Control	WiFi: CSMA/CA with ACK BT: AFH, Time Division
Antenna	External Antenna
Network Architecture	WiFi: Ad-hoc mode (Peer-to-Peer) Infrastructure mode

	Software AP WiFi Direct BT: Pico Net, Scatter Net
Security	WiFi: WPA, WPA-PSK, WPA2, WPA2-PSK, WEP 64bit & 128bit, IEEE 802.11x, IEEE 802.11i BT: Simple Paring
OS Supported	Android /Linux/ Win CE /iOS /XP/WIN7
Host Interface	WiFi: SDIO BT: UART
Operating Voltage	3.3±10% Vdc I/O supply voltage
Dimension	Typical L12.0*W12.0*H1.6mm

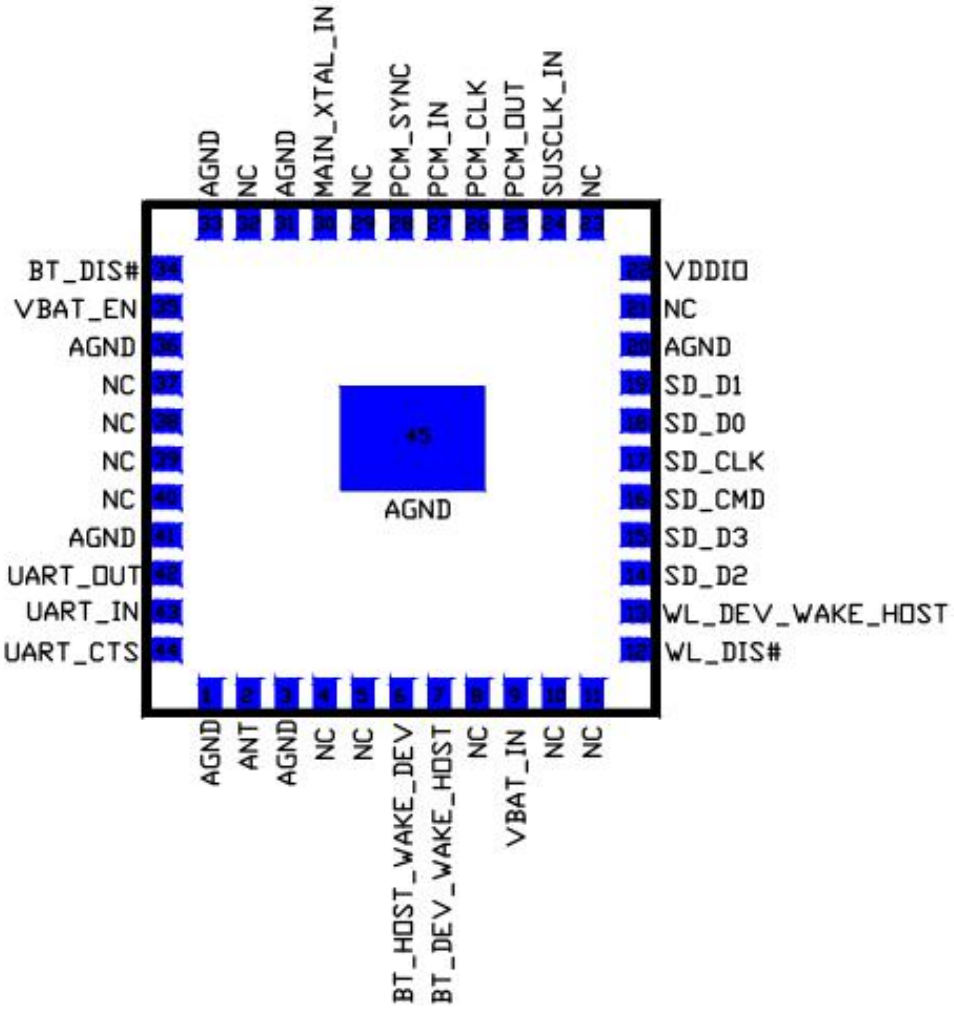
5. Power Consumption

Power Consumption (Typical by using SWR)	WiFi only: TX Mode: (Throughput mode) 170mA (MCS7/BW40/13dBm) RX Mode: (Throughput mode) 130mA (MCS7/BW40/-60dBm) Associated Idle power saving with DTIM=3 2.1mA Unassociated Idle: 0.1mA RF disable Mode: 0.1mA BT: Inquiry & Page Scan: 0.9 mA ACL no traffic: 7.5mA SCO HV3: 15.0mA

6. Pin Assignments

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition

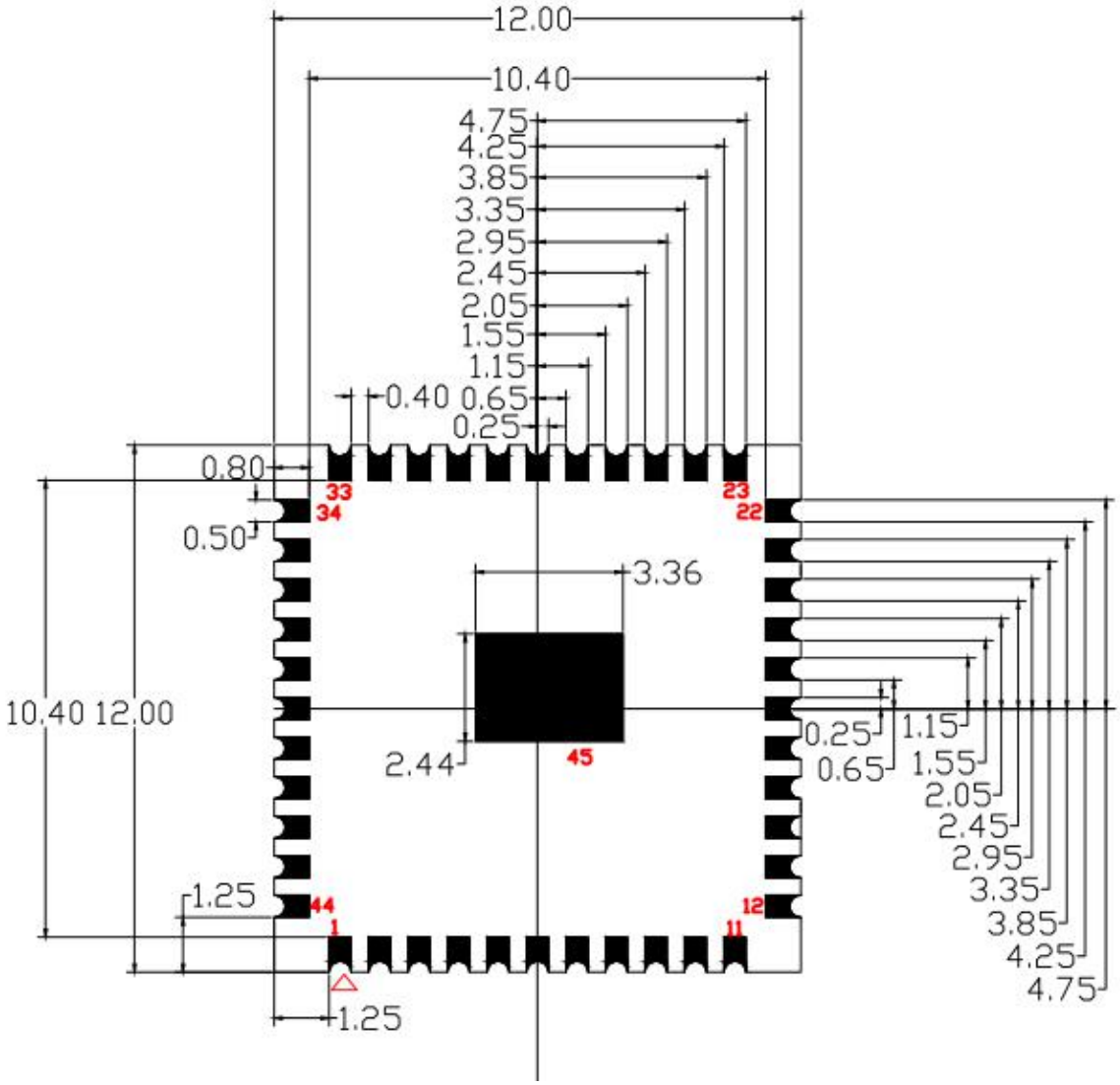
NO.	Name	Description
1	AGND	Ground connections
2	WL_BT_ANT	RF I/O port
3	AGND	Ground connections
4	NC	Floating (NC)
5	NC	Floating (NC)
6	HOST_WAKE_BT	Host to wake up Bluetooth device
7	BT_WAKE_HOST	Bluetooth device to wake up host
8	NC	Floating (NC)
9	VBAT_IN	3.3±10% V Main power voltage source input

10	NC	Floating (NC)
11	NC	Floating (NC)
12	WL_DIS#	Internal regulators power enable/disable
13	WL_HOST_WAKE	WLAN to wake up HOST
14	SD_D2	SDIO data line 2
15	SD_D3	SDIO data line 3
16	SD_CMD	SDIO command line
17	SD_CLK	SDIO clock line
18	SD_D0	SDIO data line 0
19	SD_D1	SDIO data line 1
20	AGND	Ground connections
21	NC	Floating(NC)
22	VDDIO	I/O Voltage supply input
23	NC	Floating (NC)
24	SUSCLK_IN	External Clock input(32.768kHz), need to be reserved
25	PCM_OUT	PCM Output
26	PCM_CLK	PCM Clock
27	PCM_IN	PCM Input
28	PCM_SYNC	PCM Sync
29	NC	Floating (NC)
30	MAIN_XTAL_IN	Floating (NC)
31	AGND	Ground connections
32	NC	Floating (NC)
33	AGND	Ground connections
34	BT_DIS#	BT Reset IN
35	VBAT_EN	Floating (NC)
36	AGND	Ground connections
37	NC	Floating (NC)
38	NC	Floating (NC)
39	NC	Floating (NC)
40	NC	Floating (NC)
41	UART_RTS	UART RTS
42	UART_OUT	UART Output
43	UART_IN	UART Input
44	UART_CTS	UART CTS
45	AGND	Floating (NC)

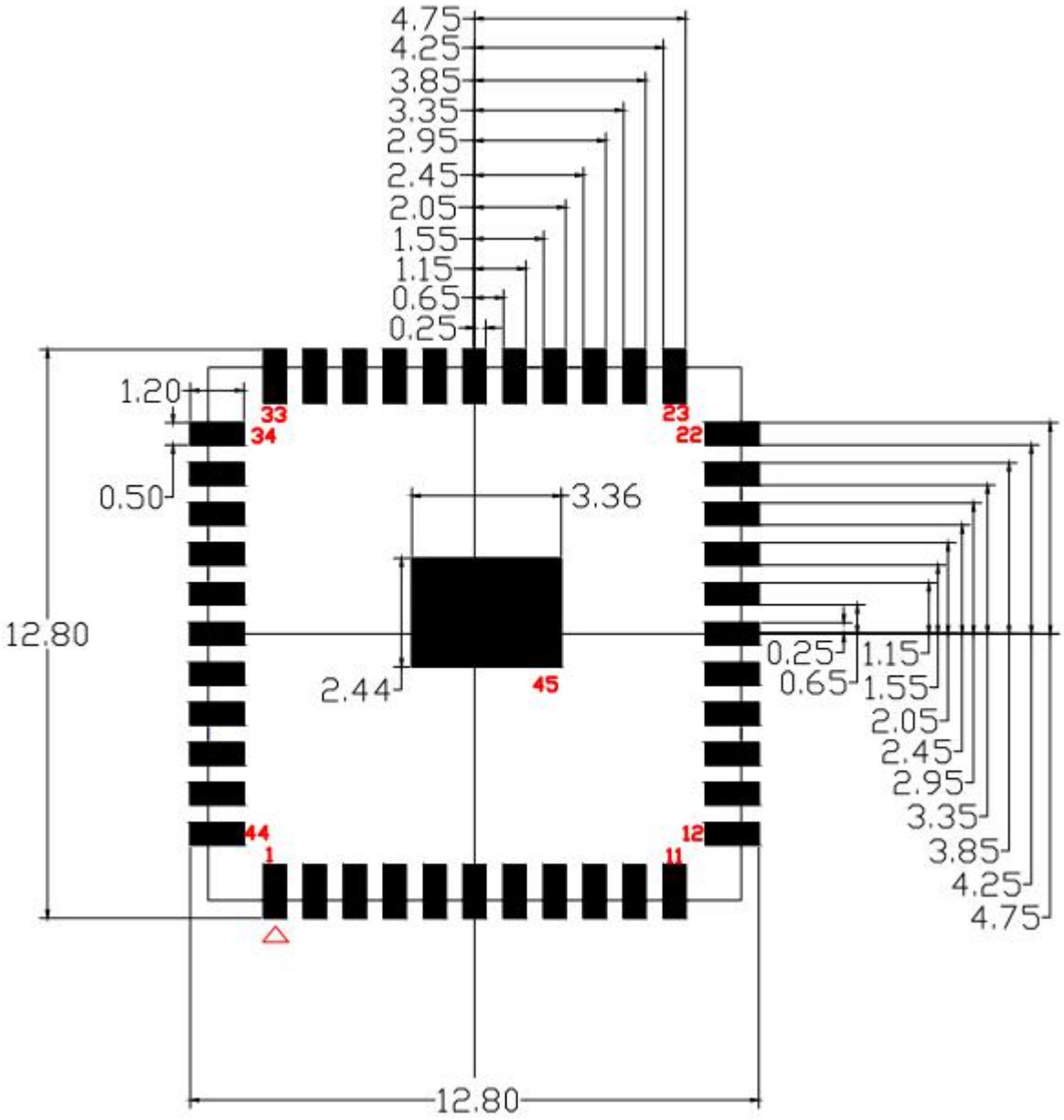
7. Dimensions

7.1 Physical Dimensions

<Bottom View>



7.2 Layout Recommendation



8. Host Interface Timing Diagram

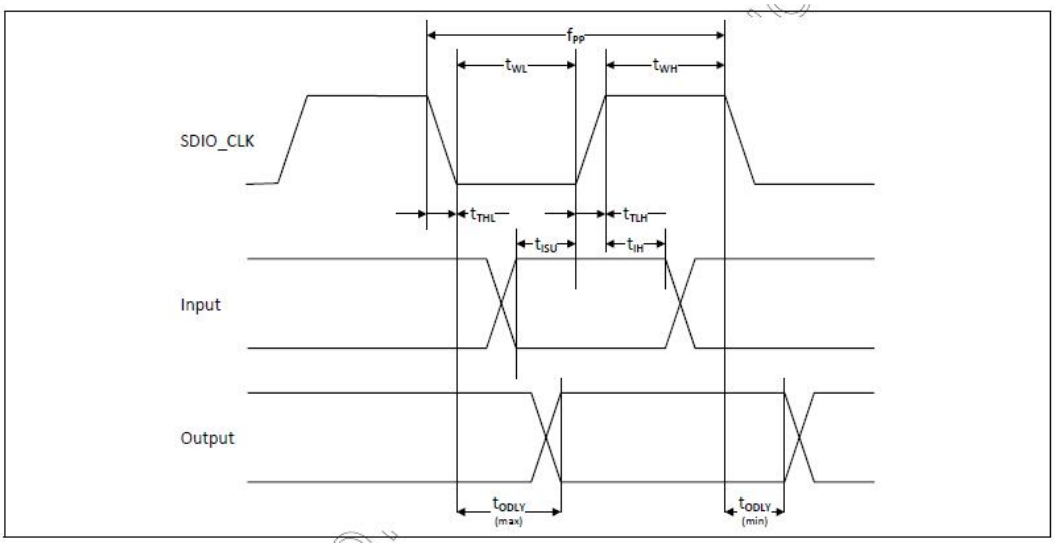
8.1 SDIO Pin Description

The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 Mbps), and DDR50(50MHz, dual rates) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

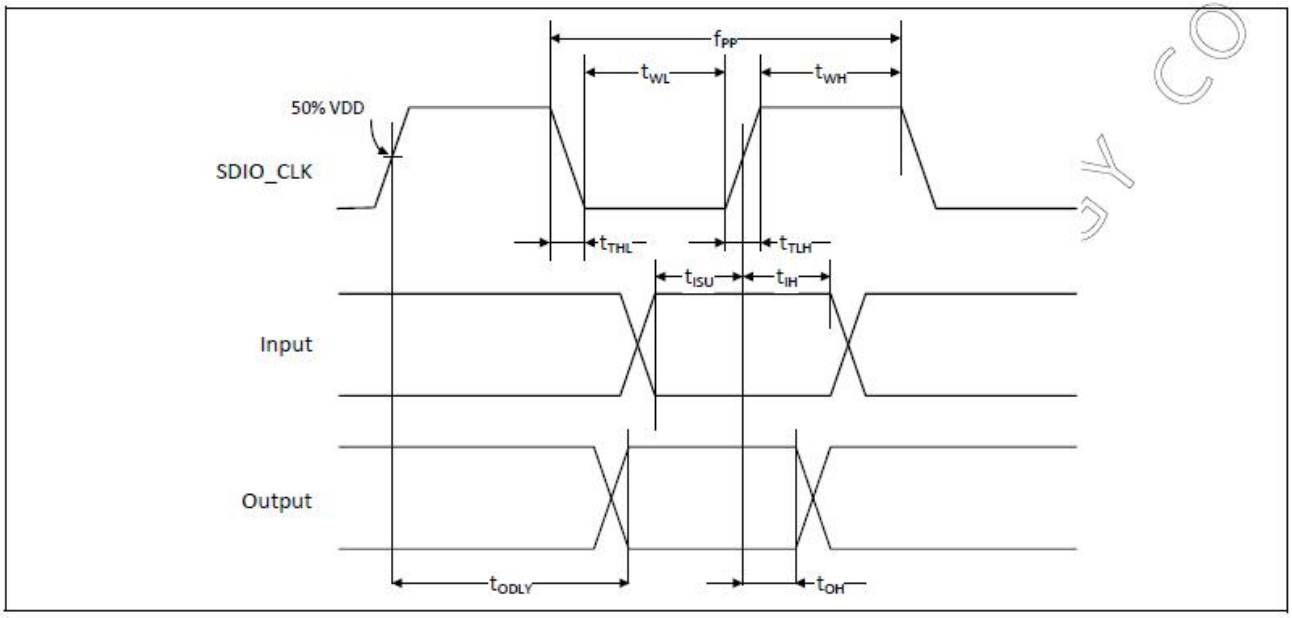
8.2 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

8.3 SDIO High Speed Mode Timing Diagram

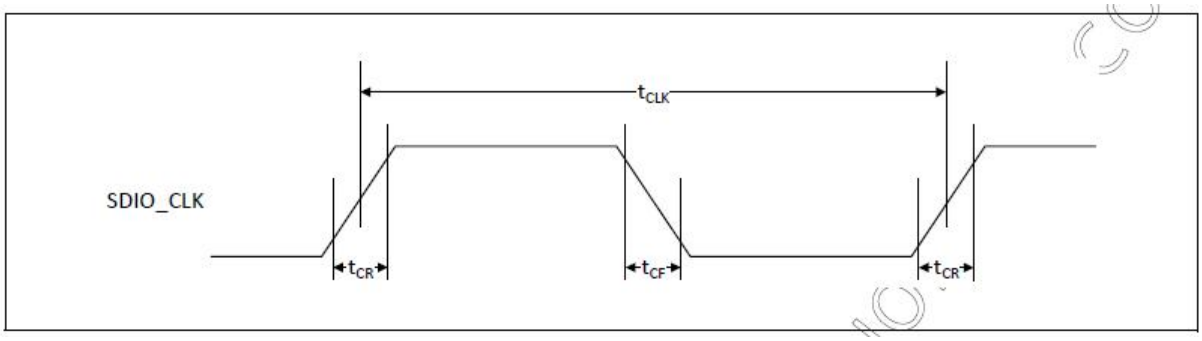


Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

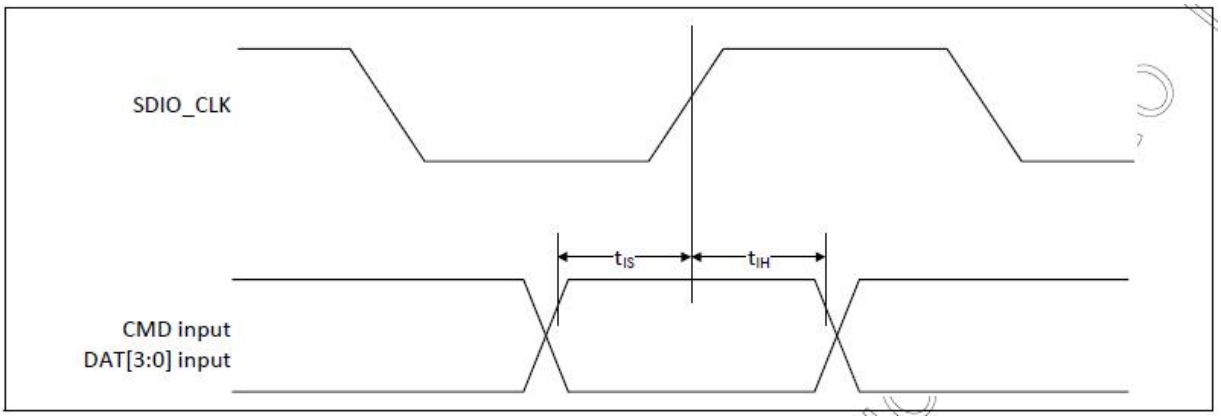
8.4 SDIO Bus Timing Specifications in SDR Modes

Clock timing(SDR Modes)



Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		10	–	ns	SDR50 mode
		4.8	–	ns	SDR104 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, C_{CARD} = 10 pF
Clock duty	–	30	70	%	–

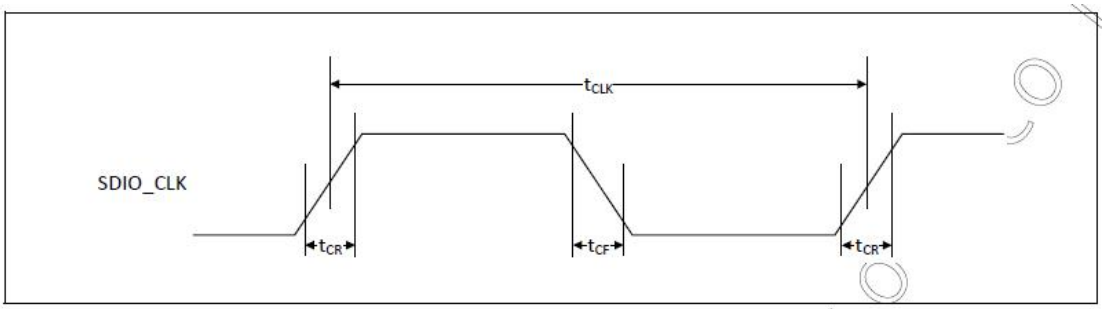
Card Input timing (SDR Modes)



Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.70[a]	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.80	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

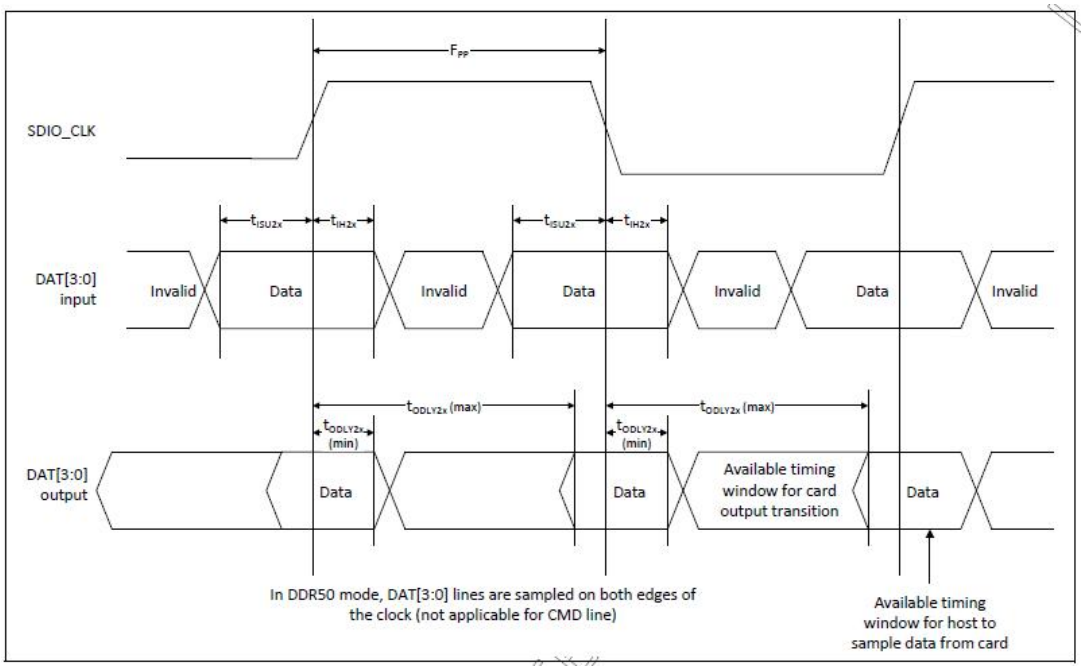
a. SDIO 3.0 specification value is 1.40 ns.

8.5 SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	20	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45	55	%	–

Data Timing



Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.85[a]	ns	C_{CARD} < 25pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15pF (1 Card)

a. SDIO 3.0 specification value is 7.0 ns.

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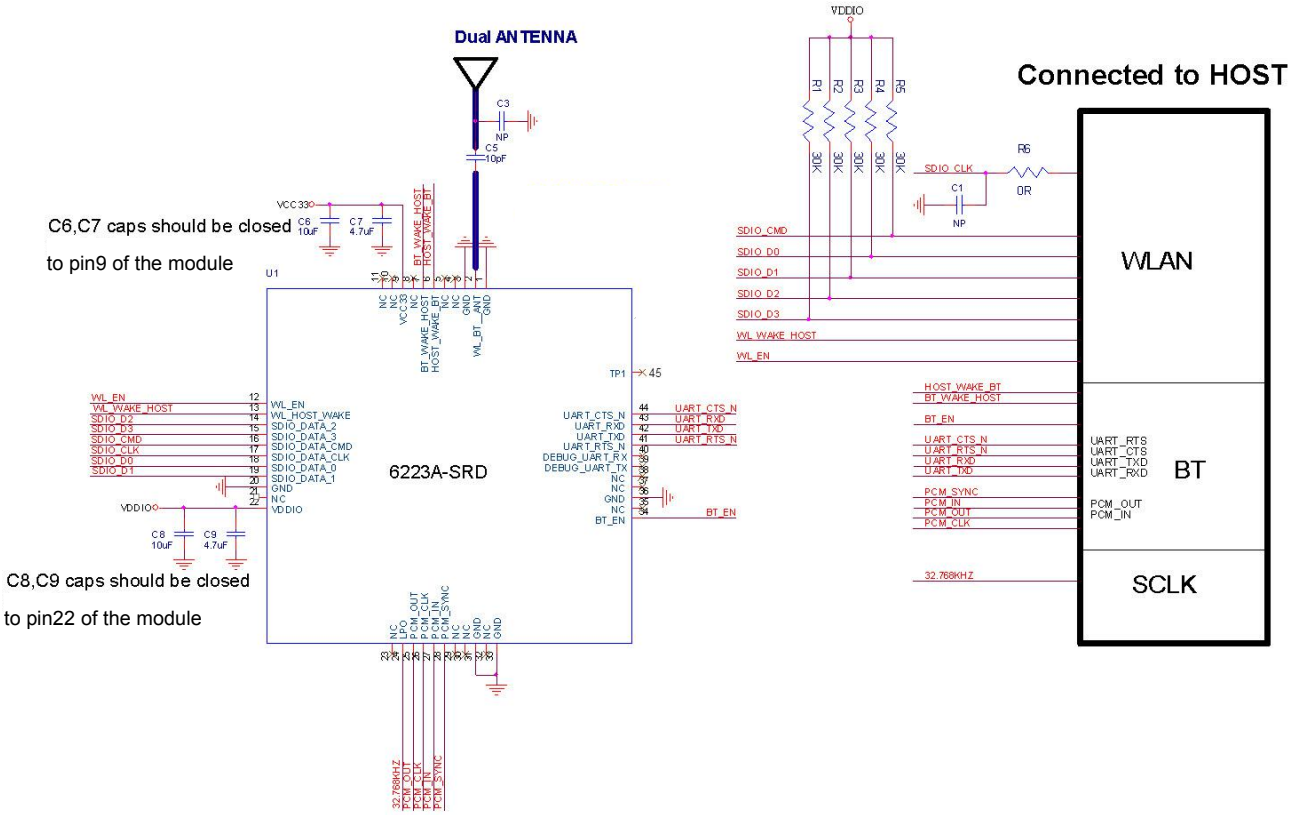
9. Reference Design



10. The Key Material List

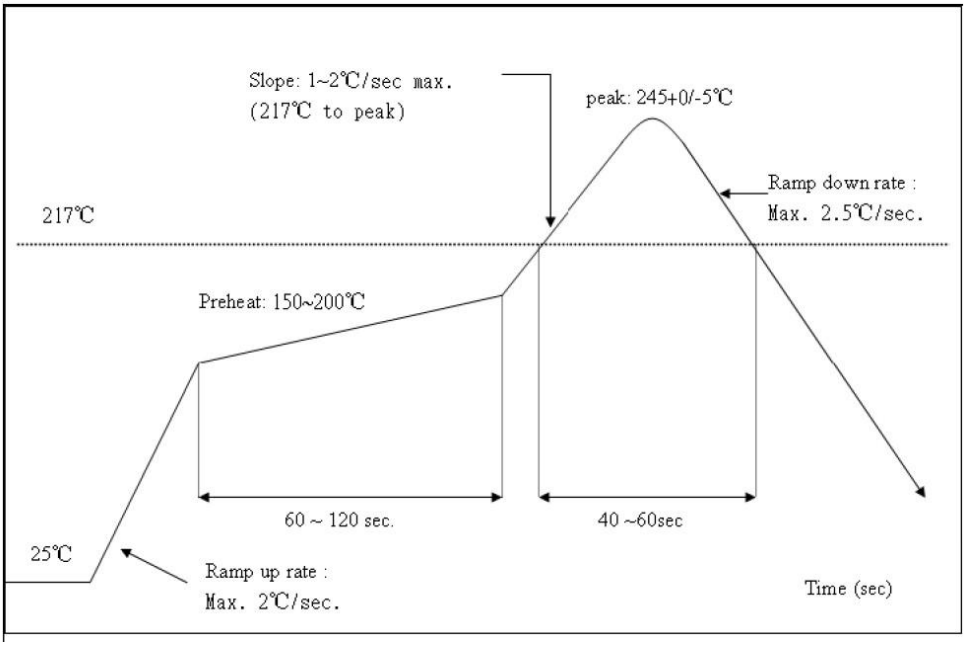
主料	主 IC	RTL8723DS_QFN48
主料	PCB	F23DSSM23_20160513　12X12X0.6mm 四层板　板材 FR4（翔宇）
主料	SMD 晶振	2520　24MHz 12pF 10ppm (TST)
替代料	SMD 晶振	2520　24MHz 12pF 10ppm　E2SB24E00000LE　Hosonic（鸿星）

11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

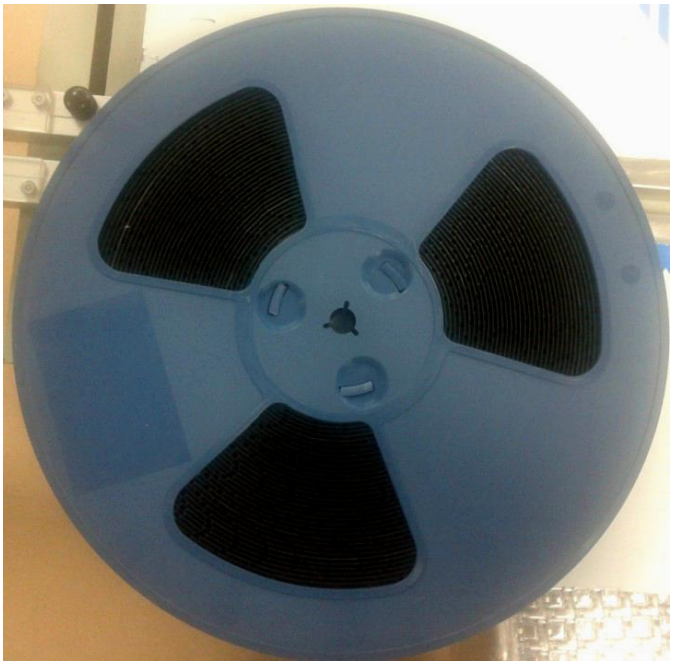
Peak Temperature : <250°C

Number of Times : ≤2 times



12. Package

the take-up package



Using self-adhesive tape
Size of black tape: 24mm*32.6m　the cover tape　:2.13mm*32.6m
Color of plastic disc: blue
A roll of 2000pcs

NY bag size:460mm*385mm

size ： 350*350*35mm

The packing case size:350*210*370mm